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Evaluation of New-Generation IGBTs for Marine Applications

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Alla mia famiglia,
per il sostegno costante, la fiducia
e la pazienza dimostrata durante questo percorso.

"The only way to do great work is to love what you do."
— Steve Jobs

Abstract

The transition from conventional internal combustion propulsion systems to electrified propulsion architectures is driving the increasing adoption of power electronic converters in marine applications. In these systems, efficiency, power density, and reliability represent key design requirements.
This thesis, carried out in collaboration with Nidec ASI S.p.A., investigates the potential replacement of the currently adopted EconoPACK+ IGBT modules with a new generation of LV100 package IGBTs while maintaining a comparable product cost.
To support this analysis, a MATLAB-based electro-thermal simulation tool was developed to evaluate semiconductor conduction losses, switching losses, and junction temperatures under operating conditions representative of the AD5000 marine drive platform. The model was validated through comparison with Infineon IPOSIM simulations and experimental double-pulse test measurements performed on the existing EconoPACK+ solution.
The validated model was then used to assess the performance of the new LV100 IGBT technology. The obtained results show that the new devices provide lower semiconductor losses and improved thermal performance, enabling either higher efficiency at the same operating current or increased current capability while maintaining comparable loss levels. Furthermore, the possibility of operating at higher switching frequencies may contribute to reducing the size of external passive components, thus increasing converter power density.
Finally, Silicon Carbide (SiC) MOSFET technology is discussed as a possible future development. Although SiC devices could further improve converter performance, their higher cost and the limited industrial experience in marine applications currently limit their adoption.

Contents

Chapter 1

Introduction

1.1 Overview of Power Electronics

Power electronics is the field of electrical engineering concerned with the conversion, control, and conditioning of electric power by means of electronic switching devices. The main objective of power electronic systems is to efficiently convert electrical energy from one form to another while maintaining high performance and reliability.

Modern power electronic converters are widely used in several applications, including renewable energy systems, electric vehicles, industrial motor drives, power supplies, and smart grids. The increasing demand for energy efficiency and high-performance electrical systems has made power electronics a key technology in modern industry.

Unlike linear power conversion techniques, power electronic converters operate semiconductor devices mainly in switching mode. This approach allows the reduction of power dissipation and improves overall efficiency. Typical switching devices include power diodes, MOSFETs, and IGBTs, each characterized by different voltage, current, and switching capabilities.

Power converters can be classified into four main categories: AC/DC rectifiers, DC/DC converters, DC/AC inverters, and AC/AC converters. Among these, voltage source inverters play a fundamental role in applications requiring the generation of controlled AC voltages from a DC power source.

In addition to power semiconductor devices, modern power electronic systems include control units, sensing circuits, gate drivers, and passive components such as capacitors and inductors. The correct interaction between these elements is essential to achieve stable operation, high efficiency, and reduced electromagnetic interference.

The following sections introduce the architecture and operating principles of a two-level three-phase voltage source inverter, together with the main switching

devices and modulation techniques commonly adopted in industrial applications.

1.2 Inverter Architecture

A voltage source inverter is a power electronic converter designed to generate an AC output voltage starting from a DC power source. The inverter operation is based on the controlled switching of semiconductor devices, which allows the synthesis of variable voltage and frequency waveforms suitable for different applications [1].

Modern inverter systems are composed of several hardware blocks that work together to ensure correct operation, high efficiency, and reliable control. The main components typically include the control logic, the DC-link capacitor stage, the power switching devices, sensing circuits, and the gate driver boards. The control unit is responsible for generating the modulation signals and managing the overall inverter operation. The DC-link capacitors stabilize the input DC voltage and reduce voltage ripple caused by the switching activity. The power semiconductor devices perform the actual power conversion process by rapidly switching the current flow according to the selected modulation strategy.

Current and voltage sensors provide feedback information required for regulation, protection, and monitoring purposes. Finally, the gate driver boards interface the low-power control circuitry with the high-power semiconductor switches, ensuring proper isolation and fast switching performance.

The interaction between these subsystems strongly influences the overall inverter behavior in terms of efficiency, switching losses, thermal stress, and output waveform quality. For this reason, the design of inverter architecture represents a fundamental aspect in modern power electronic systems.

1.2.1 Control Logic

The control logic represents the central unit of the inverter system and is typically implemented using a microcontroller, a digital signal processor (DSP), or a field-programmable gate array (FPGA). Its main function is to manage the switching operation of the power semiconductor devices in order to generate the desired output voltage and frequency.

The controller executes the modulation algorithms used to produce the gate signals for the inverter switches. Common modulation techniques include Sinusoidal Pulse Width Modulation (SPWM) and Space Vector Modulation (SVM), which allow the synthesis of sinusoidal output waveforms with reduced

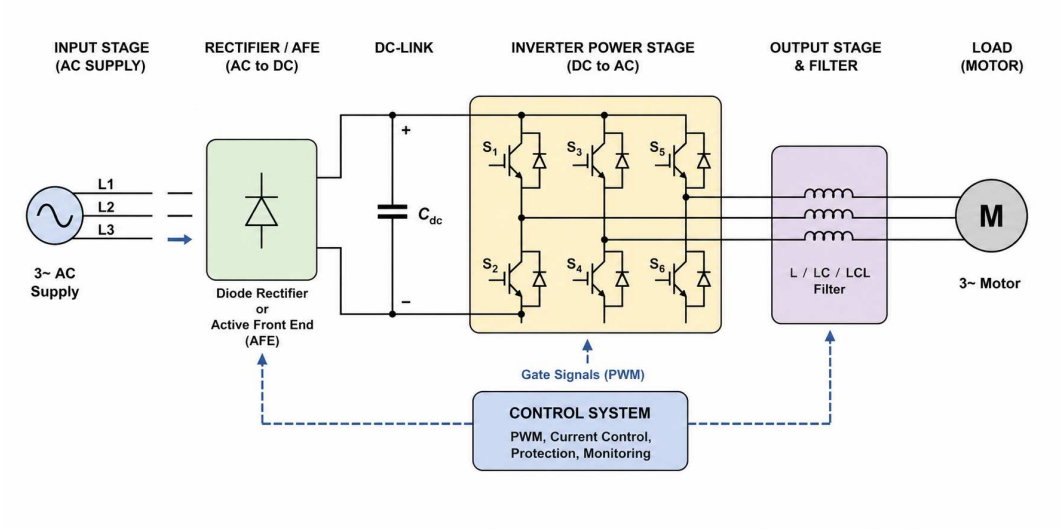

Figure 1.1: Typical scheme of an inverter used as motor drive.

harmonic distortion [2].

In addition to modulation tasks, the control unit performs several monitoring and protection functions. Current and voltage measurements acquired from the sensing circuits are processed in real time to regulate the inverter operation and prevent abnormal conditions such as overcurrent, overvoltage, or overheating. Modern microcontrollers used in power electronics applications integrate high-speed analog-to-digital converters (ADCs), PWM peripherals, communication interfaces, and dedicated protection features. These integrated peripherals simplify the implementation of real-time control algorithms and improve the overall reliability of the system.

The computational capability of the controller directly affects the achievable switching frequency, control bandwidth, and dynamic response of the inverter. For this reason, the selection of the control platform depends on the complexity and performance requirements of the specific application.

1.2.2 DC-link Capacitors

DC-link capacitors are fundamental components in voltage source inverters and are placed between the DC power source and the switching stage. Their main purpose is to stabilize the DC-link voltage and provide temporary energy storage during the inverter operation.

During the switching process, the inverter draws pulsating currents from the DC source. Without proper filtering, these current variations would produce significant voltage ripple on the DC bus, negatively affecting the converter performance and the output waveform quality. DC-link capacitors reduce these voltage fluctuations by supplying or absorbing energy according to the instantaneous power demand.

Another important function of the DC-link capacitor stage is the decoupling between the input source and the inverter switching operation. This improves system stability and reduces the propagation of high-frequency disturbances toward the power supply.
The selection of the capacitor technology depends on the electrical and thermal requirements of the application. Electrolytic capacitors are commonly used because of their high capacitance values and relatively low cost, while film capacitors provide lower equivalent series resistance (ESR), improved high-frequency performance, and longer operational lifetime.
The capacitor sizing process must consider several parameters, including DC voltage level, ripple current, switching frequency, thermal stress, and expected lifetime. An insufficient capacitance value may lead to excessive voltage ripple and reduced system reliability, whereas oversized capacitors increase cost and physical dimensions.
In high-power inverter applications, multiple capacitors are often connected in parallel in order to distribute the ripple current and improve thermal performance.

1.2.3 Power Switching Stage

The power switching stage represents the core of the inverter and is responsible for the conversion of electrical energy from DC to AC form. This stage is composed of semiconductor switching devices arranged in a specific converter topology, typically a three-phase bridge configuration in industrial applications.
The inverter output voltages are generated through the controlled switching of the semiconductor devices. By properly activating and deactivating the switches according to the selected modulation strategy, the converter synthesizes AC waveforms with controlled amplitude and frequency.
The switching devices operate at high frequencies in order to improve the quality of the output waveform and reduce harmonic distortion. However, higher switching frequencies also increase switching losses and thermal stress, requiring a careful design trade-off between efficiency and waveform performance.
The power stage must withstand high voltage and current levels during operation. For this reason, the selection of the semiconductor devices strongly depends on the application requirements, including power rating, switching frequency, thermal constraints, and efficiency targets.
Proper layout design and minimization of parasitic inductances are also important aspects of the switching stage. Excessive parasitic elements may generate voltage overshoots, electromagnetic interference, and additional switching

losses.

1.2.4 Current and Voltage Sensors

Current and voltage sensors are essential components in inverter systems because they provide the feedback signals required for control, monitoring, and protection functions.

Voltage measurements are typically used to monitor the DC-link voltage and the inverter output voltages. Current sensing is instead fundamental for motor control applications, power regulation, and overcurrent protection.

Several sensing technologies can be adopted depending on the required accuracy, bandwidth, isolation level, and cost. Current measurements are commonly performed using shunt resistors, Hall-effect sensors, or current transformers. Voltage sensing is generally implemented through resistive divider networks combined with isolation circuits when necessary.

The measured signals are acquired by the analog-to-digital converters of the control unit and processed in real time by the control algorithms. Accurate measurements are particularly important in closed-loop control systems, where the quality of the feedback signals directly affects system stability and dynamic performance.

In addition to regulation purposes, sensing circuits also contribute to the implementation of protection mechanisms. Fast detection of abnormal operating conditions allows the controller to disable the switching devices and protect the inverter against possible failures.

1.2.5 Gate Driver Boards

Gate driver boards provide the interface between the low-power control logic and the high-power semiconductor switching devices. Their main function is to generate the gate signals required to properly turn the power devices on and off.

Since semiconductor switches such as MOSFETs and IGBTs require specific voltage and current levels for correct operation, the microcontroller outputs cannot directly drive the devices. Gate drivers amplify the control signals and provide the necessary current to rapidly charge and discharge the gate capacitances [3].

Fast switching transitions are important to reduce switching losses, but excessively high switching speed may increase electromagnetic interference and voltage overshoots. For this reason, gate driver circuits are carefully designed to achieve a suitable compromise between efficiency and switching behavior.

In many inverter applications, galvanic isolation between the control stage and the power stage is required for safety and noise immunity reasons. Isolation can be achieved through pulse transformers or opto-isolators integrated within the driver circuitry.
Modern gate driver boards integrate several advanced protection and control functions in addition to basic signal amplification. These features are designed to improve switching performance, increase system reliability, and protect the power semiconductor devices against abnormal operating conditions.
Among the most common protection mechanisms are undervoltage lockout (UVLO), desaturation detection, soft shutdown, and active Miller clamp circuits. While UVLO prevents the device from operating with insufficient gate voltage, desaturation protection detects excessive collector-emitter voltage during conduction, which may indicate a short-circuit event. Soft shutdown circuits are used to safely turn off the device during fault conditions, reducing overvoltage stress caused by excessive current transients [4].
Particular importance is given to the active Miller clamp, which has become a standard feature in modern IGBT and SiC MOSFET gate driver solutions.

Active Miller Clamp During fast switching transitions, the collector-emitter voltage of an IGBT can change rapidly, generating significant displacement currents through the parasitic gate-collector capacitance, commonly referred to as the Miller capacitance.
The current generated by this capacitive coupling may produce an unwanted increase of the gate-emitter voltage in the complementary switch of the inverter leg. If the induced gate voltage exceeds the device threshold voltage, an unintended turn-on event may occur. This phenomenon is commonly known as parasitic turn-on and may lead to increased switching losses, electromagnetic interference, or even shoot-through conditions.
To prevent this issue, modern gate drivers often implement an active Miller clamp circuit. When the gate voltage falls below a predefined threshold during turn-off, an internal transistor creates a low-impedance connection between the gate and emitter terminals. This additional current path prevents the gate voltage from rising due to Miller current injection and maintains the device in a safe off-state [4].
Compared to the use of negative gate voltages alone, the Miller clamp provides an effective and compact solution for high-power applications operating with high switching speeds and large dv/dt values.

1.3 Power Semiconductor Devices

Power semiconductor devices are the key components that enable energy conversion in modern power electronic systems. These devices operate mainly as electronic switches, alternating between conduction and blocking states in order to control the power flow with high efficiency [1].
The ideal switching device should present zero voltage drop during conduction, infinite resistance in the off-state, and instantaneous switching transitions. In practical applications, however, semiconductor devices exhibit conduction losses, switching losses, and limited operating speed.
Different types of power semiconductor devices are available, each characterized by specific electrical and thermal performances. The selection of the most suitable device depends on the converter topology, switching frequency, voltage rating, current capability, and efficiency requirements.
Among the most widely used devices in inverter applications are power diodes, MOSFETs, and Insulated Gate Bipolar Transistors (IGBTs). Their operating principles and characteristics are discussed in the following sections.

1.3.1 Power Diodes

Power diodes are semiconductor devices that allow current conduction only in one direction. They are among the simplest and most widely used power electronic components and are commonly employed in rectifiers, freewheeling paths, and protection circuits.
A power diode operates in forward bias when the anode voltage is higher than the cathode voltage, allowing current flow through the device. Under reverse bias conditions, the diode blocks the current until the breakdown voltage is reached.
Unlike low-power signal diodes, power diodes are specifically designed to withstand high current and voltage levels. However, they present non-ideal characteristics such as forward voltage drop and reverse recovery effects.
The reverse recovery phenomenon occurs when the diode transitions from conduction to blocking state. During this interval, a reverse current flows through the device due to the removal of stored charge carriers. Reverse recovery contributes to switching losses and may generate electromagnetic interference and voltage overshoots.
Different types of power diodes are available, including standard recovery diodes, fast recovery diodes, and Schottky diodes. Fast recovery devices are preferred in high-frequency applications because of their reduced reverse recovery time, while Schottky diodes provide very low forward voltage drop and

negligible recovery losses at lower voltage ratings.

1.3.2 MOSFETs

The Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) is a voltage-controlled semiconductor device widely used in low- and medium-power converters operating at high switching frequencies.
The MOSFET conduction mechanism is based on majority carriers only, allowing very fast switching operation and reduced switching losses. The device is controlled through the gate terminal, which is electrically insulated from the semiconductor structure by a thin oxide layer. As a consequence, the gate current required during steady-state operation is practically negligible.
Power MOSFETs are characterized by low switching times, simple gate drive requirements, and excellent high-frequency performance. For these reasons, they are commonly used in DC/DC converters, switching power supplies, and low-voltage motor drive applications.
One of the main limitations of MOSFETs is the increase of the on-state resistance with higher voltage ratings. This causes higher conduction losses in high-power and high-voltage applications.
The intrinsic body diode of the MOSFET also plays an important role in inverter operation, especially during freewheeling intervals. However, the reverse recovery characteristics of the body diode may affect the switching performance in some applications.

1.3.3 IGBTs

The Insulated Gate Bipolar Transistor (IGBT) combines the advantages of MOSFET gate control with the high-current capability of bipolar devices. It is one of the most widely used semiconductor devices in medium- and high-power inverter applications.
Like the MOSFET, the IGBT is controlled by voltage applied to the insulated gate terminal, resulting in relatively simple gate drive requirements. However, the conduction mechanism involves both majority and minority charge carriers, allowing lower conduction losses at high voltage levels compared to power MOSFETs.
IGBTs are particularly suitable for applications operating at medium switching frequencies and high power levels, such as industrial motor drives, renewable energy converters, traction systems, and uninterruptible power supplies.
Despite slower switching performance than MOSFETs, IGBTs provide excellent voltage and current capabilities, making them the preferred solution in many high-power applications above several kilowatts.

Internal Structure

As previously mentioned, the IGBT combines the gate structure of a power MOSFET with the current conduction mechanism of a bipolar transistor. The simplified equivalent circuit consists of an N-channel MOSFET controlling the base current of a PNP transistor.

Physically, the device is composed of four semiconductor layers forming a PNPN structure. The collector side is typically realized using a heavily doped P+ substrate, while the emitter side consists of an N+ region controlled through an insulated gate electrode. Between the collector and emitter regions, a lightly doped drift region provides the voltage-blocking capability required in high-power applications.

The injection of minority carriers into the drift region significantly reduces the on-state resistance, resulting in lower conduction losses compared to high-voltage MOSFETs. This phenomenon, known as conductivity modulation, is one of the key advantages of the IGBT technology.

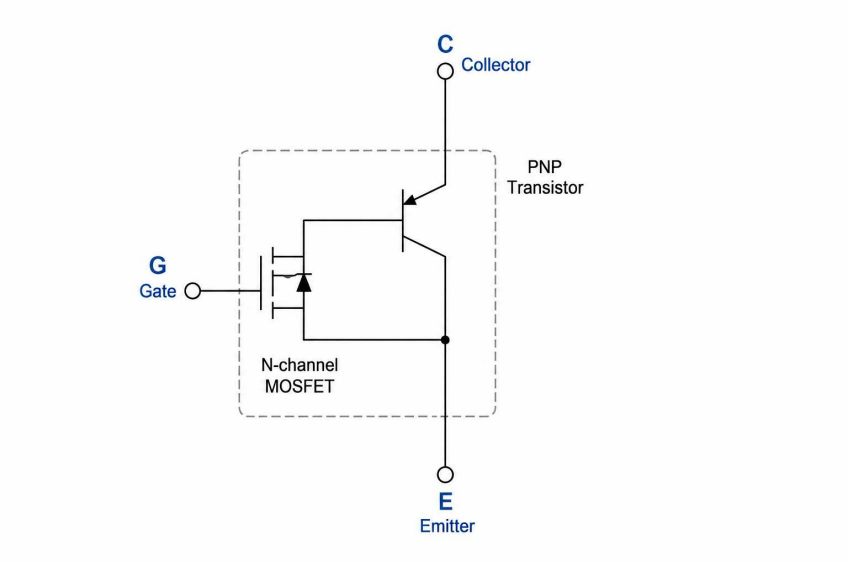

Figure 1.2: Simplified IGBT equivalent structure.

Operating Principle

The operation of the IGBT can be divided into three main states: blocking, turn-on, and conduction.

When the gate-emitter voltage is below the threshold voltage, no conductive channel is formed beneath the gate oxide and the device remains in the blocking state. In this condition, the IGBT is capable of sustaining high collector-emitter voltages while only a very small leakage current flows through the device.

When a positive gate-emitter voltage exceeding the threshold value is applied, an inversion channel is created in the MOSFET portion of the device. Electrons begin to flow from the emitter toward the drift region, activating the internal PNP transistor. As a result, holes are injected from the collector side into the drift region, establishing bipolar conduction.

During the conduction state, both electrons and holes contribute to current transport. The presence of minority carriers reduces the resistance of the drift region, leading to a relatively low collector-emitter voltage drop even at high current levels. This allows the IGBT to achieve lower conduction losses than a comparable high-voltage MOSFET.

When the gate voltage is removed, the MOS channel disappears and the device begins turning off. However, the minority carriers stored in the drift region cannot be removed instantaneously. These stored charges continue contributing to current flow for a short period of time, producing the characteristic current tail observed during the turn-off transient .

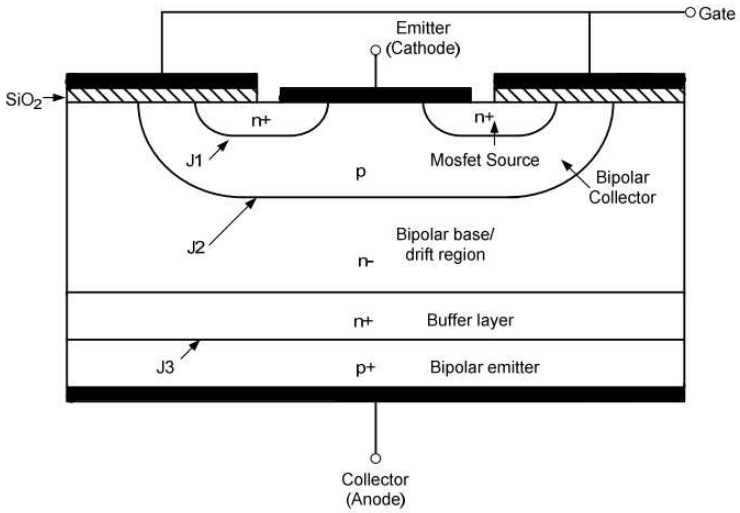

Figure 1.3: Physical structure of an IGBT power device.

Static Characteristics

The static behaviour of an IGBT is commonly described through its output and transfer characteristics. The output characteristic represents the relationship between collector current and collector-emitter voltage for different values of gate-emitter voltage. Once the device is fully enhanced, the collector-emitter voltage remains relatively low and can be approximated by the on-state voltage drop $V_{CE(sat)}$. The transfer characteristic describes the dependence of collector current on gate-emitter voltage. Above the threshold voltage, the collector current increases rapidly as the gate voltage increases. The exact shape of the characteristic depends on device technology, junction temperature, and operating conditions.

The on-state voltage drop is one of the most important static parameters because it directly influences the conduction losses of the device. Higher current levels generally result in larger conduction losses and increased thermal stress.

Dynamic Characteristics

The dynamic behaviour of the IGBT is determined by the charging and discharging processes of its internal capacitances and by the storage of minority carriers within the semiconductor structure.

During switching transitions, the device exhibits finite turn-on and turn-off times. The gate-emitter and gate-collector capacitances influence the switching speed and contribute to the appearance of the Miller plateau in the gate voltage waveform .

During turn-on, the collector current rises while the collector-emitter voltage decreases from the DC-link voltage to the on-state voltage drop. During turn-off, the opposite process occurs. Since voltage and current overlap during these transitions, energy is dissipated inside the semiconductor.

The switching performance of an IGBT is typically characterized by the turn-on energy E_{on}, the turn-off energy E_{off}, and the reverse recovery energy associated with the freewheeling diode. These parameters are commonly provided by semiconductor manufacturers and are extensively used for switching loss estimation and thermal analysis.

Limitations and Challenges

Despite their widespread use, IGBTs present several limitations.

One of the main drawbacks is the current tail phenomenon observed during turn-off transitions. The stored minority carriers within the drift region continue contributing to current flow after the gate voltage has been removed, increasing switching losses and limiting the maximum switching frequency.

Another limitation is the relatively slow switching speed compared to power MOSFETs. For this reason, IGBTs are generally preferred in medium-frequency applications, while MOSFETs and SiC MOSFETs are often selected for very high switching frequencies.
The switching behaviour is also influenced by parasitic capacitances and stray inductances present in the power circuit. These parasitic elements may generate voltage overshoots, increased electromagnetic interference, and unwanted device stress during fast switching transitions .
Finally, thermal management plays a critical role in high-power applications. Excessive junction temperatures may reduce reliability and accelerate device degradation. Therefore, careful heatsink design, cooling system optimization, and thermal analysis are essential to guarantee safe and reliable converter operation.

1.4 Switching Transients and Power Losses

Power semiconductor devices do not switch instantaneously between the on-state and off-state conditions. During switching transitions, voltage and current coexist across the device, generating power dissipation and thermal stress. Power losses in semiconductor devices can be mainly divided into conduction losses and switching losses. These losses strongly affect converter efficiency, cooling requirements, and device reliability.
The analysis of switching transients is therefore fundamental for the design of high-performance power electronic converters. Switching behavior depends on several factors, including device technology, gate driving conditions, parasitic inductances, and operating current levels.
Accurate estimation of semiconductor losses is essential for thermal design and efficiency optimization in inverter systems.

1.4.1 Turn-on and Turn-off Transients (IGBT)

The dynamic behaviour of an IGBT is strongly influenced by its internal capacitances, carrier storage effects, and interactions with the external circuit. Unlike an ideal switch, the device requires a finite amount of time to transition between the blocking and conduction states, resulting in switching losses.
The switching behaviour described in this section is adapted from the analysis presented in [6].
Figure 1.4 shows the simplified equivalent circuit commonly adopted to describe the dynamic behaviour of an IGBT. The model includes the main parasitic capacitances, namely the gate-emitter capacitance C_{ge}, the gate-collector

capacitance C_{gc} (also known as Miller capacitance), and the collector-emitter capacitance C_{ce}. Furthermore, the parasitic inductances associated with the collector and emitter connections are taken into account through L_c and L_e.

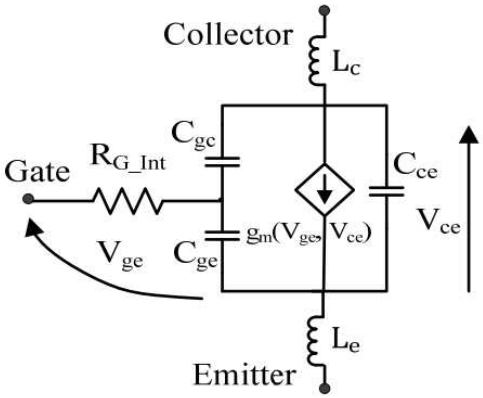

Figure 1.4: Simplified equivalent circuit model of an IGBT including internal capacitances and parasitic inductances, adapted from [6].

The values of the internal capacitances are not constant but strongly depend on the collector-emitter voltage. As shown in Fig. 1.5, the Miller capacitance C_{gc} exhibits a significant variation with V_{CE}, particularly at low voltages. This non-linear behaviour plays a fundamental role during switching transitions, especially during the Miller plateau interval.

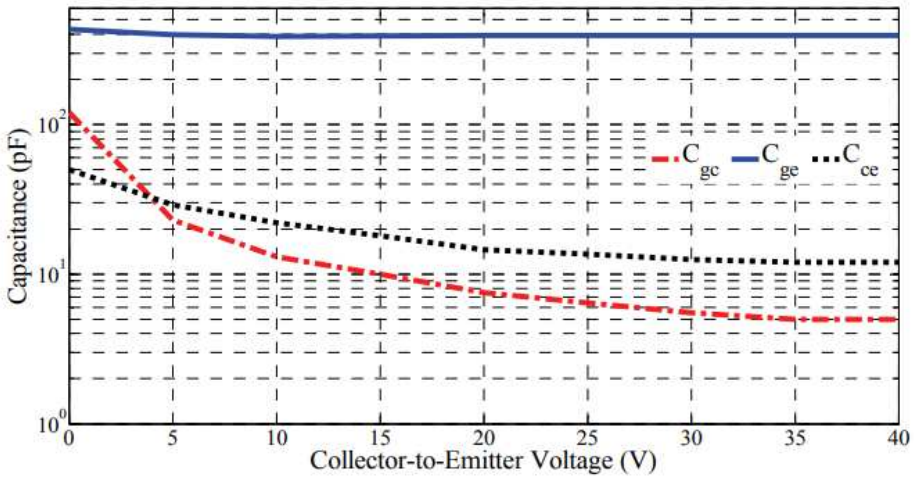

Figure 1.5: Typical variation of the IGBT internal capacitances as a function of collector-emitter voltage, adapted from [6].

A typical turn-on transient is reported in Fig. 1.6. The switching process can be divided into different operating phases. Initially, during the turn-on delay interval, the gate capacitances are charged until the threshold voltage is reached, while no significant variation of collector current is observed. Once the threshold is exceeded, the collector current starts increasing and the current

previously flowing through the freewheeling diode is progressively transferred to the IGBT.

As the collector current reaches the load current value, the freewheeling diode enters reverse recovery, producing a temporary current overshoot. Subsequently, the collector-emitter voltage rapidly decreases during the Miller plateau interval while the gate voltage remains almost constant. This region is characterized by the simultaneous presence of significant voltage and current across the device and therefore represents the major contribution to the turn-on switching energy E_{on}.

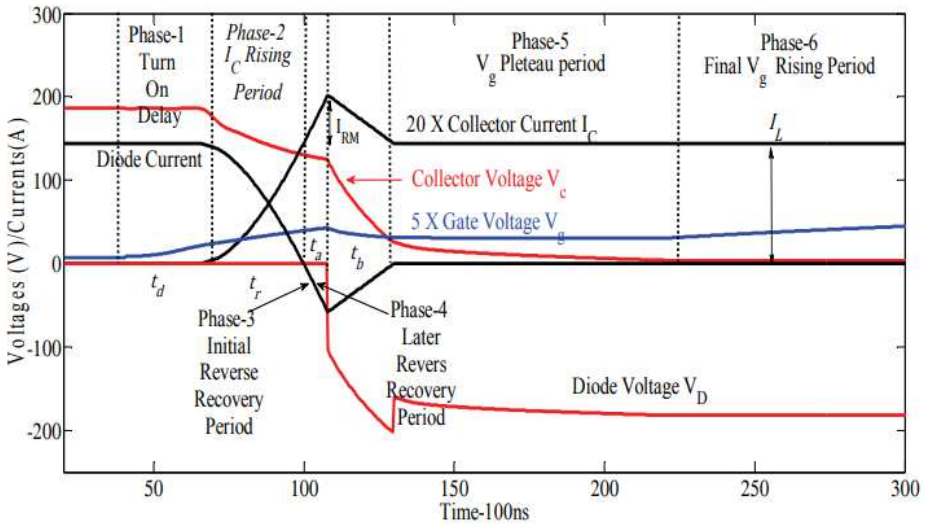

Figure 1.6: Typical IGBT turn-on transient highlighting the different switching phases and the evolution of current and voltage waveforms, adapted from [6].

During turn-off, the opposite process takes place. A typical turn-off transient is illustrated in Fig. 1.7. Initially, after the removal of the gate command, the gate-emitter voltage starts decreasing during the turn-off delay interval, while the collector current remains almost constant.

Once the Miller plateau is reached, the collector-emitter voltage rapidly increases toward the DC-link voltage. During this interval, the gate current is mainly employed to charge the Miller capacitance C_{gc} and the device simultaneously supports both significant voltage and current, thus generating the majority of the turn-off switching energy E_{off}.

After the voltage transition is completed, the collector current starts decreasing. Due to the presence of stored minority carriers within the drift region, the current does not immediately vanish but exhibits a characteristic tail current. This phenomenon, known as *current tail*, is intrinsic to IGBT technology and represents one of the main factors limiting the maximum achievable switching frequency, since it contributes significantly to the turn-off losses.

The duration of the tail current strongly depends on junction temperature

and device technology. Modern trench field-stop IGBTs considerably reduce this effect compared with previous generations, allowing improved switching performance and lower losses.
A more detailed discussion regarding the influence of gate resistance and parasitic inductances on the measured waveforms will be presented in Chapter 4 during the analysis of the experimental results.

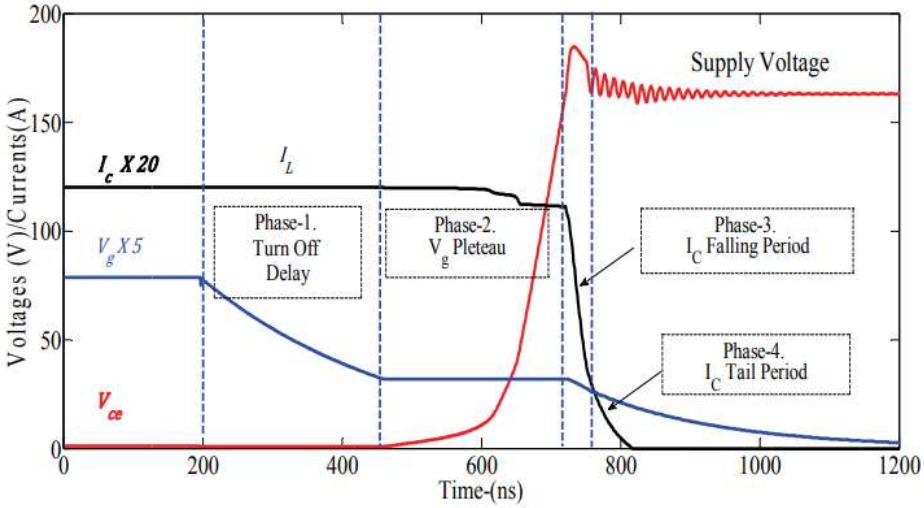

Figure 1.7: Typical IGBT turn-off transient showing the turn-off delay, Miller plateau, collector current fall and tail current periods, adapted from [6].

1.4.2 Conduction Losses

Conduction losses are generated when the semiconductor device operates in the on-state and conducts current. These losses depend on the voltage drop across the device and the current flowing through it.
In power diodes and IGBTs, conduction losses are mainly associated with the forward voltage drop of the semiconductor junction. In MOSFETs, instead, conduction losses are determined by the drain-source on-state resistance $R_{DS(on)}$.
The average conduction power loss can generally be expressed as:

$$P_{cond} = V_{on} \cdot I_{avg}$$

for devices characterized by an approximately constant voltage drop, or as:

$$P_{cond} = I_{rms}^2 \cdot R_{DS(on)}$$

for MOSFET devices.
Conduction losses increase with current and temperature and contribute significantly to the thermal stress of the semiconductor devices.

1.4.3 Switching Losses

Switching losses are generated during the turn-on and turn-off transitions of semiconductor devices. Unlike conduction losses, switching losses strongly depend on the switching frequency.
The switching energy dissipated during each transition can be approximated by the overlap between device voltage and current waveforms. The average switching power loss is commonly expressed as:

$$P_{sw} = (E_{on} + E_{off}) \cdot f_{sw}$$

where E_{on} and E_{off} are the turn-on and turn-off energies, and f_{sw} is the switching frequency [1].
Higher switching frequencies improve the output waveform quality and reduce the size of passive components, but they also increase switching losses and thermal stress.
Switching losses are particularly important in high-frequency converters and often represent the main limitation in the selection of the operating switching frequency.

1.4.4 Thermal Modelling of Power Semiconductor Devices

During the operation of power semiconductor devices, conduction and switching losses generate heat inside the semiconductor chip, leading to an increase of the junction temperature T_j. Since the electrical characteristics, efficiency and lifetime of IGBT modules are strongly affected by temperature, an accurate estimation of the thermal behaviour represents an important aspect in the design and validation of high-power converters.
The thermal behaviour of a power module can be described using an equivalent thermal network, based on the analogy between thermal and electrical quantities. The dissipated power corresponds to an electrical current source, the temperature difference corresponds to voltage, while thermal resistance and thermal capacitance are represented by electrical resistors and capacitors respectively.
The transient thermal response of the device is usually described through the thermal impedance Z_{th}, which defines the temperature variation produced by a power variation over time:

$$Z_{th}(t) = \frac{\Delta T(t)}{P}$$

Two main equivalent RC networks are commonly used for semiconductor thermal modelling: the Cauer network and the Foster network [12].
The Cauer model represents the physical structure of the semiconductor module. Each RC stage is associated with a specific layer of the heat propagation path, such as silicon chip, solder layer, substrate, baseplate and heatsink. Therefore, this approach is particularly useful when the temperature distribution inside the package has to be analysed.
On the other hand, the Foster model is a mathematical representation obtained by fitting the transient thermal impedance curve of the device. Unlike the Cauer approach, the single RC elements do not correspond to physical layers of the module, but the complete network accurately reproduces the dynamic thermal response between the junction and the reference temperature.
The Foster thermal impedance can be expressed as:

$$Z_{th}(t) = \sum_{i=1}^{n} R_i \left(1 - e^{-\frac{t}{R_i C_i}}\right)$$

where R_i and C_i represent the thermal resistance and capacitance of each equivalent RC branch.
Although the Cauer model provides a more physical representation of the heat flow, manufacturers commonly provide Foster coefficients in power module datasheets, since they can be directly extracted from experimental transient thermal impedance measurements [12].
For this reason, the Foster thermal network was selected in this work. This choice allows the thermal parameters provided by the semiconductor manufacturer to be directly implemented into the electro-thermal simulation tool without requiring additional conversion procedures.
The detailed MATLAB implementation of the Foster network will be presented in Section 3.5.

1.5 Two-Level Three-Phase Voltage Source Inverter

The two-level three-phase Voltage Source Inverter (VSI) is one of the most common converter topologies used in modern power electronics applications. It is widely adopted in industrial motor drives, renewable energy systems, electric vehicles, and uninterruptible power supplies because of its relatively simple structure and high reliability [1].
The converter consists of three inverter legs connected to a common DC-link voltage source. Each leg contains two controlled semiconductor switches op-

erating in a complementary manner in order to avoid short-circuiting the DC bus. The midpoint of each leg forms one phase output of the inverter.

By controlling the switching states of the semiconductor devices, the inverter generates three-phase AC voltages from the DC input source. In a two-level topology, each phase output can assume only two possible voltage levels with respect to the DC-link midpoint: positive or negative DC voltage.

The switching states of the inverter are determined by the modulation strategy implemented by the control unit. Proper switching sequences allow the synthesis of approximately sinusoidal output voltages and currents suitable for AC loads and electric machines.

The simplicity of the two-level VSI topology provides several advantages, including reduced circuit complexity, lower cost, and easier control implementation. However, the generated output voltage contains switching harmonics that may require filtering and can increase electromagnetic interference.

The performance of the inverter strongly depends on the selected semiconductor devices, switching frequency, modulation technique, and DC-link voltage level. For this reason, accurate design and optimization of the inverter parameters are essential to achieve high efficiency and good output waveform quality.

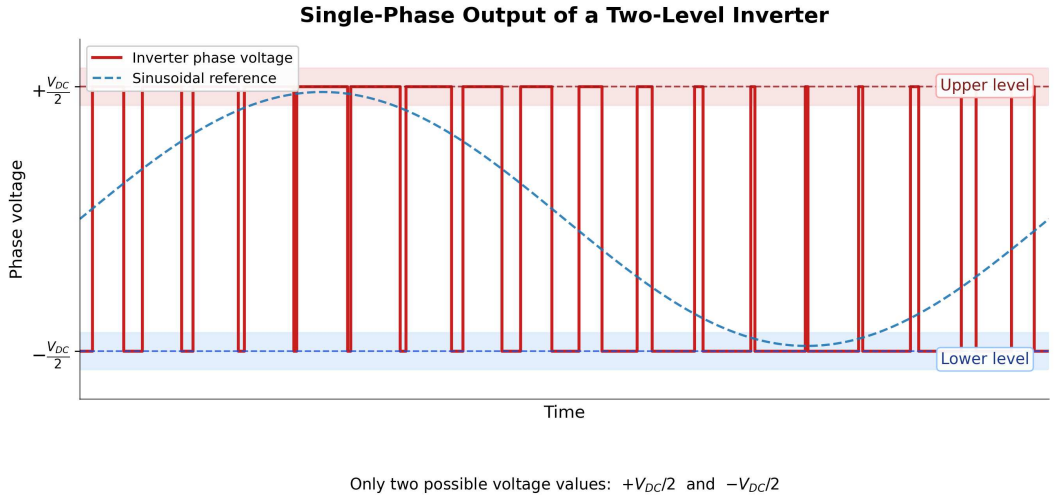

Figure 1.8: Single-phase output voltage of a two-level inverter. The phase voltage can assume only two discrete levels, $+V_{DC}/2$ and $-V_{DC}/2$.

1.6 Modulation Techniques

Modulation techniques are fundamental in voltage source inverters because they determine the switching sequence of the semiconductor devices and directly influence the output voltage quality, harmonic content, switching losses, and overall converter efficiency [2].

The objective of the modulation process is to synthesize AC output waveforms with controlled amplitude and frequency starting from a fixed DC voltage source. This is achieved by properly controlling the switching instants of the inverter power devices.

Different modulation strategies have been developed for inverter applications, each characterized by specific advantages and limitations in terms of harmonic distortion, computational complexity, DC bus utilization, and switching performance.

Among the most commonly used modulation methods for two-level three-phase inverters are Sinusoidal Pulse Width Modulation (SPWM) and Space Vector Modulation (SVM). These techniques are widely adopted in industrial applications because they provide good waveform quality and relatively simple implementation.

1.6.1 Sinusoidal PWM (SPWM)

Sinusoidal Pulse Width Modulation (SPWM) is one of the simplest and most widely used modulation techniques for voltage source inverters. The method is based on the comparison between a low-frequency sinusoidal reference signal and a high-frequency triangular carrier waveform [2].

When the sinusoidal reference is greater than the carrier signal, the upper switch of the inverter leg is turned on. Conversely, when the carrier waveform exceeds the reference signal, the lower switch is activated. This process generates a sequence of voltage pulses whose average value follows the sinusoidal reference waveform.

The amplitude and frequency of the inverter output voltage can be controlled by modifying the amplitude and frequency of the reference sinusoidal signals. In three-phase systems, three sinusoidal references shifted by 120° are used.

SPWM offers several advantages, including simple implementation, predictable harmonic spectrum, and relatively low computational requirements. However, the technique presents limited DC bus voltage utilization compared to more advanced modulation methods.

The harmonic performance of SPWM depends on the switching frequency and modulation index. Increasing the switching frequency improves the output

waveform quality but also increases switching losses in the semiconductor devices.

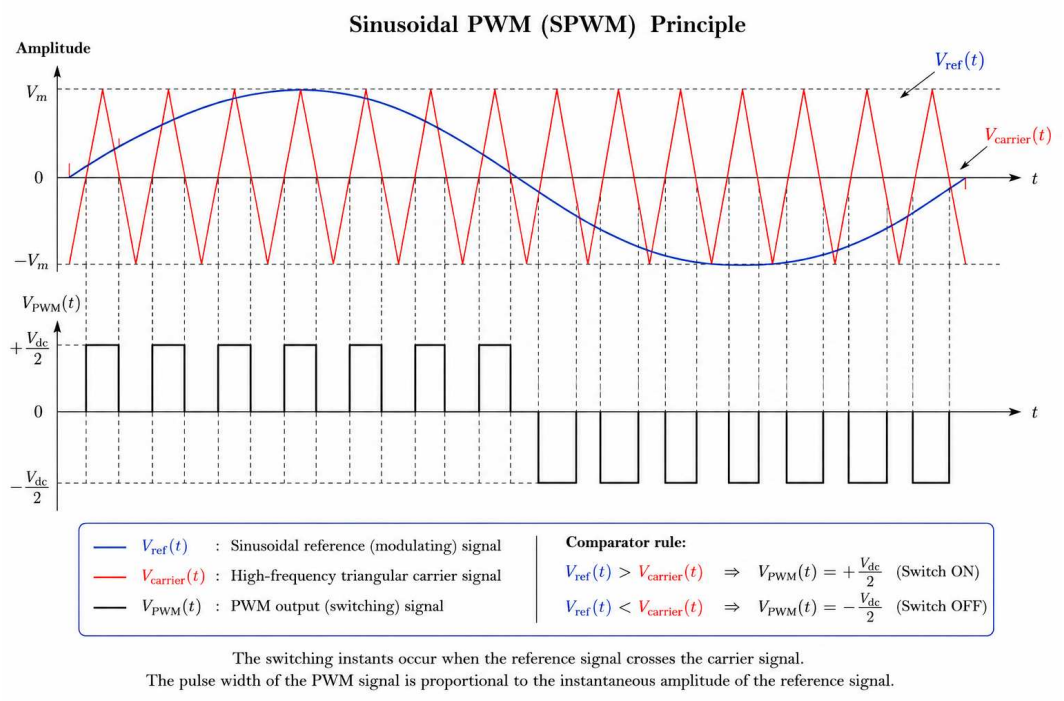

Figure 1.9: Sinusoidal PWM principle.

1.6.2 Space Vector Modulation (SVM)

Space Vector Modulation (SVM) is an advanced modulation technique commonly used in three-phase voltage source inverters. Compared to traditional SPWM, SVM provides improved DC bus voltage utilization and reduced harmonic distortion.

The basic principle of SVM is the representation of the three-phase inverter voltages as a single rotating voltage vector in a two-dimensional plane. Depending on the switching states of the inverter, different voltage vectors can be generated.

In a two-level three-phase inverter, eight possible switching combinations are available. Six of these combinations generate active voltage vectors, while the remaining two correspond to zero vectors.

During each switching period, the reference voltage vector is synthesized by combining adjacent active vectors and zero vectors for appropriate time intervals. This approach allows the inverter to approximate the desired sinusoidal output voltage with high accuracy.

One of the main advantages of SVM is the improved utilization of the DC-link voltage, which is approximately 15% higher than that achievable with

conventional SPWM. In addition, SVM generally produces lower harmonic distortion and better switching performance.

Despite its higher computational complexity, modern digital controllers allow efficient real-time implementation of SVM algorithms, making this technique widely adopted in high-performance inverter applications.

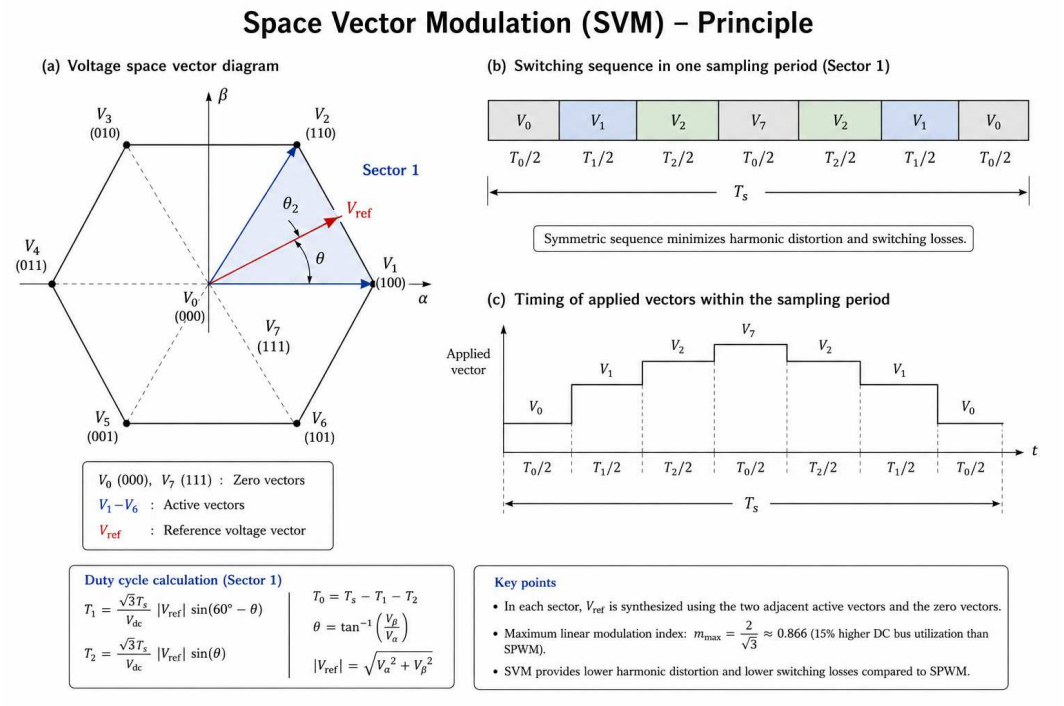

Figure 1.10: Space Vector Modulation principle.

Chapter 2

Marine Applications and State of the Art

2.1 Applications of Power Inverters in Industrial Systems

Power inverters are widely used in modern industrial systems due to their capability to efficiently control electric power conversion and electric machine operation. The development of high-performance semiconductor devices and digital control systems has significantly increased the diffusion of inverter-based solutions in several industrial sectors . One of the most important applications of power inverters is variable speed motor control. In industrial automation systems, inverters allow precise regulation of motor speed and torque, improving process flexibility, energy efficiency, and overall system performance. Typical applications include pumps, compressors, conveyor systems, fans, and machine tools. Power inverters are also extensively adopted in renewable energy systems such as photovoltaic and wind power plants. In these applications, the inverter converts the generated DC power into AC power compatible with the electrical grid while ensuring proper synchronization and power quality. Another important field is electric transportation, including railway systems, electric vehicles, and marine propulsion applications. In these systems, power converters are required to manage high power levels with high efficiency and reliability while operating under demanding environmental conditions. Modern industrial inverters integrate advanced control algorithms, protection systems, communication interfaces, and monitoring functions. These features allow improved system automation, predictive maintenance, and fault diagnosis capabilities. The continuous demand for higher efficiency, reduced dimensions, and lower operating costs is driving the development of new converter topologies and advanced semiconductor technologies.

2.2 Marine Propulsion Systems

Marine propulsion systems are responsible for generating the mechanical power required to move ships and marine vessels. Traditionally, propulsion systems were mainly based on mechanical transmission architectures directly coupled to diesel engines. However, the increasing demand for fuel efficiency, reduced emissions, and improved operational flexibility has accelerated the adoption of electric propulsion technologies. Modern electric and hybrid marine propulsion systems commonly employ variable speed drives and high-power inverters to control propulsion motors. In these architectures, electrical energy generated by diesel generators, batteries, or hybrid power sources is converted and regulated by power electronic converters before being supplied to the propulsion motors. The use of inverter-fed propulsion systems offers several advantages compared to conventional mechanical solutions. Variable speed operation allows improved energy efficiency, optimized fuel consumption, reduced mechanical stress, and lower acoustic noise. In addition, electric propulsion systems provide greater flexibility in ship layout and improved maneuverability. Marine applications impose particularly demanding operating conditions on power electronic converters. Marine inverters must operate reliably under high humidity, vibration, thermal stress, and limited cooling conditions. Furthermore, high reliability and fault tolerance are essential because failures may compromise vessel safety and operational continuity. Typical marine propulsion architectures include fixed-speed diesel-electric systems, fully electric propulsion systems, and hybrid propulsion configurations integrating batteries and energy storage systems. The selection of the propulsion topology depends on vessel size, power requirements, operational profile, and efficiency targets.
The growing interest in sustainable maritime transportation is promoting the development of more efficient inverter technologies and advanced semiconductor devices for marine applications.

2.3 State of the Art of Marine Inverters

Modern marine propulsion systems require high-performance power converters capable of handling large power levels with high reliability and efficiency. Several manufacturers have developed advanced inverter platforms specifically designed for marine and industrial applications. State-of-the-art marine inverters integrate advanced cooling systems, modular power structures, digital control platforms, and high-performance semiconductor devices. The main design objectives include efficiency improvement, reduction of system dimensions, simplified maintenance, and enhanced reliability under harsh environ-

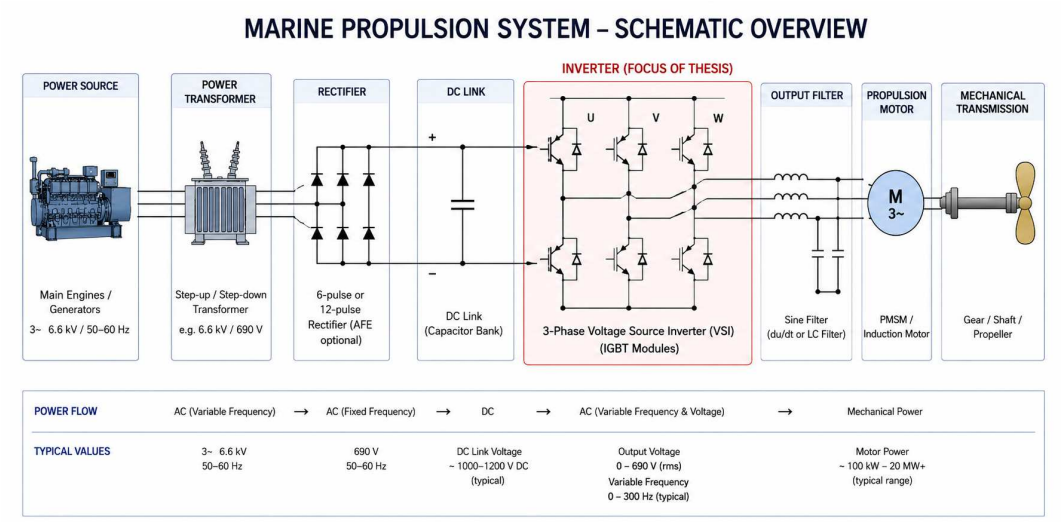

Figure 2.1: Simplified marine electric propulsion architecture.

mental conditions. Among the most relevant commercial solutions currently available on the market are the Nidec AD5000, the Danfoss iC7 series, and the ABB ACS880 platform [16, 17, 18]. These inverter families represent advanced industrial solutions for medium- and high-power applications and provide different design approaches in terms of modularity, switching technology, cooling architecture, and control implementation. The following sections present an overview of these inverter platforms and compare their main technical characteristics.

2.3.1 Nidec AD5000

The Nidec AD5000 is a low-voltage industrial inverter designed for medium- and high-power applications requiring high reliability, modularity, and ease of maintenance [16]. The drive is available in several voltage classes ranging from 380 V to 690 V and can provide power ratings up to 4 MW through the parallel connection of multiple power modules.

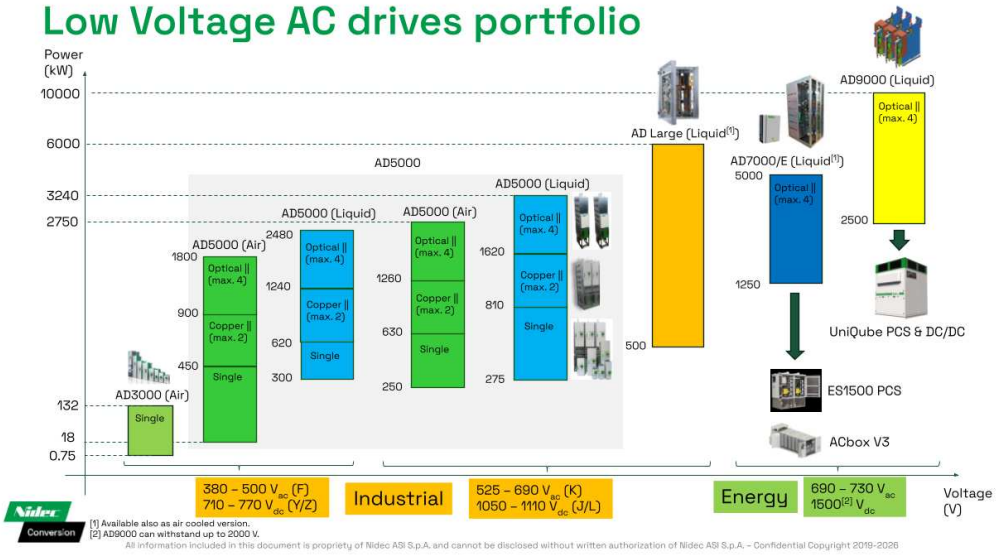

Figure 2.2: Nidec AD5000 converter lineup.

The AD5000 is based on a modular architecture in which the power stage and the control system are physically separated. Communication between the control unit and the power modules is achieved through optical fiber links, providing galvanic isolation and improved immunity to electromagnetic interference.

One of the key features of the AD5000 platform is its scalability. Individual power modules can be connected in parallel to increase the output power while maintaining a modular structure and simplifying maintenance operations. In the event of a module failure, the defective unit can be replaced independently, reducing system downtime.

The converter is available in both standard inverter and Active Front End (AFE) configurations. The AFE version enables bidirectional power flow, regenerative operation, reduced harmonic distortion, and near-unity power factor, making it particularly suitable for applications with frequent braking cycles or weak electrical networks, such as marine power systems.

For the present thesis, the reference converter is the AD5W740L liquid-cooled configuration belonging to the 690 V_{AC} navy class. As shown in Fig. 2.3, this configuration is characterized by a default switching frequency of 2 kHz

and a nominal output current of 680 A_{RMS}. These values are used as the baseline operating conditions for the electro-thermal simulations presented in Chapter 3.

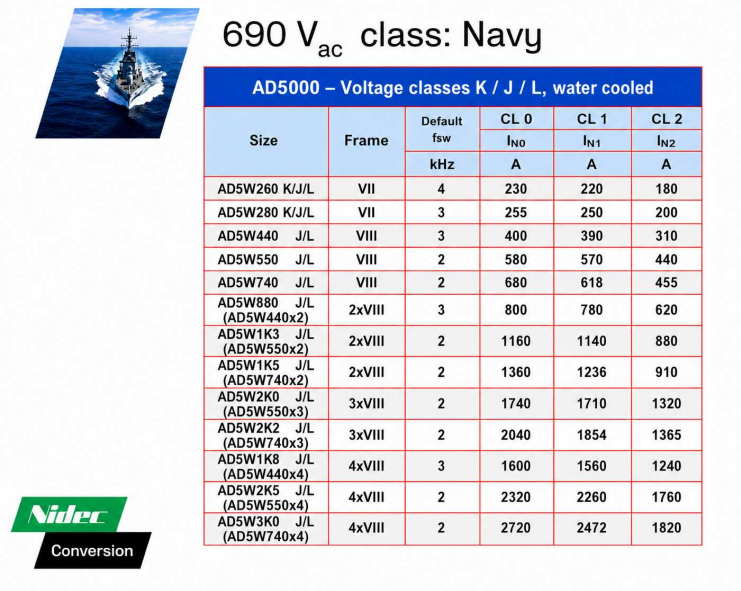

Figure 2.3: AD5000 water-cooled voltage class lineup

Due to its high power density, modular design and flexibility, the AD5000 is widely employed in demanding industrial sectors including mining, metals processing, renewable energy systems, oil and gas, and marine propulsion applications.

Figure 2.4: Nidec AD5000 cabinet layout.

2.3.2 Danfoss iC7

The Danfoss iC7-Marine is a next-generation low-voltage drive platform specifically developed for marine propulsion, thrusters, winches, and other demanding maritime applications [17]. The converter is designed to provide high power density, advanced motor control performance, and simplified system integration while meeting the stringent reliability requirements of the marine industry. One of the most distinctive features of the iC7-Marine platform is its extremely compact design. Thanks to its high power density and liquid-cooled architecture, the converter requires significantly less installation space than conventional marine drives, allowing a reduction in electrical room dimensions and cooling requirements. This characteristic is particularly attractive in marine applications, where available space is often limited. The converter is available in several voltage classes ranging from 380 V to 690 V and supports output currents up to several kiloamperes, enabling power ratings from hundreds of kilowatts to multiple megawatts. The modular architecture allows the system to be scaled according to the application requirements while maintaining a compact footprint and simplified maintenance procedures. A key aspect of the iC7 platform is the extensive integration of intelligence and sensing capabilities. Numerous embedded sensors continuously monitor the operating conditions of the converter, improving control performance, protection functions, and diagnostic capabilities. The drive also incorporates advanced motor control algorithms capable of delivering excellent torque and speed regulation, particularly at low-speed operating conditions. The iC7-Marine platform supports both inverter and Active Front End (AFE) configurations. The AFE implementation enables regenerative operation, bidirectional power flow, improved grid compatibility, and reduced harmonic distortion. These characteristics make the converter particularly suitable for modern electric and hybrid-electric marine propulsion systems. Another important feature of the iC7 series is its cybersecurity-oriented design. Hardware-based security mechanisms, encrypted communications, and compliance with modern industrial cybersecurity standards are integrated directly into the control architecture. This approach improves system reliability and helps protect critical marine infrastructure from unauthorized access. Due to its combination of compact dimensions, modular architecture, advanced motor control, and high efficiency, the Danfoss iC7-Marine represents one of the most advanced commercial solutions currently available for marine propulsion applications.

2.3.3 ABB ACS880

The ABB ACS880 is a high-performance industrial drive platform designed for a wide range of variable-speed applications, including marine propulsion, process industries, mining, oil and gas, metals processing, and renewable energy systems [18]. The drive is part of ABB's all-compatible drive family and is recognized for its flexibility, reliability, and advanced control capabilities. The ACS880 is available in both low-voltage and medium-power configurations, covering a broad power range from a few kilowatts up to several megawatts. Its modular architecture allows the drive to be adapted to different installation requirements while simplifying maintenance and system expansion. A key feature of the ACS880 platform is the Direct Torque Control (DTC) technology developed by ABB. Unlike conventional vector control methods, DTC directly controls motor torque and flux without requiring a pulse encoder in many applications. This approach enables fast dynamic response, accurate speed control, and excellent performance over a wide operating range. The converter can be configured with either a diode rectifier or an Active Front End (AFE). The AFE configuration enables regenerative operation, bidirectional power flow, low harmonic distortion, and near-unity power factor, making the drive suitable for demanding marine and industrial applications where energy efficiency and grid compliance are critical requirements. The ACS880 incorporates advanced protection and monitoring functions, including condition monitoring, fault diagnostics, thermal supervision, and predictive maintenance features. These capabilities improve system availability and reduce maintenance costs throughout the converter lifetime. The drive platform also supports multiple communication protocols and automation interfaces, facilitating integration within modern industrial control systems and shipboard power management architectures. Due to its high reliability, advanced motor control capabilities, and scalable modular design, the ABB ACS880 has become one of the most widely adopted industrial drive solutions for high-power applications, including electric and hybrid marine propulsion systems. For marine propulsion applications, the ACS880 is frequently employed in propulsion drives, thrusters, pumps, compressors, and auxiliary power systems, where high efficiency, operational reliability, and precise motor control are essential requirements.

2.3.4 Comparison of Technical Specifications

The comparison between the Nidec AD5000, the Danfoss iC7-Marine and the ABB ACS880 shows that all three platforms are suitable for demanding medium- and high-power industrial applications. They support low-voltage inverter operation, modular architectures, advanced control functions and, de-

pending on the configuration, Active Front End operation. The Nidec AD5000 is characterized by a modular structure and high scalability. According to the manufacturer, the converter can reach power ratings up to 4 MW at 690 V through the parallel connection of multiple power modules. The platform is designed to simplify installation and maintenance, and the separation between control and power modules through optical fiber connections improves galvanic isolation and noise immunity. However, during the analysis of the converter architecture, one of the main limitations identified for the AD5000 is related to the overall system footprint. Although the AD5000 is presented by the manufacturer as a compact solution for its class, newer drive platforms show a stronger focus on power density and space reduction. This aspect is particularly relevant in marine applications, where the available space inside the electrical room is limited and the converter volume directly affects installation flexibility. The Danfoss iC7-Marine represents a more recent design approach, with a strong emphasis on compactness, liquid cooling and high power density. The manufacturer highlights the possibility of reducing the drive footprint compared to traditional solutions, making the platform particularly attractive for marine propulsion systems where space and weight are critical design constraints. The ABB ACS880, on the other hand, is mainly characterized by its industrial maturity, wide power range and advanced motor control capabilities. Its Direct Torque Control strategy and extensive range of cabinet and module configurations make it a highly flexible solution for industrial and marine applications. From this comparison, the AD5000 does not appear to be limited by power capability, modularity or application flexibility. Its main disadvantage, when compared with more recent converter platforms, is instead related to the physical size and power density of the overall system, both in air-cooled and water-cooled configurations. This observation provides one of the motivations for investigating new-generation semiconductor devices, since lower losses and improved thermal performance may allow a reduction in cooling requirements, cabinet size and total converter footprint.

2.4 Internal Architecture of the Nidec AD5000

The Nidec AD5000 is a drive platform developed for demanding industrial and marine applications [16]. Its architecture is designed to ensure high reliability, modularity, and effective thermal management while operating at high power levels.

The converter is composed of several functional subsystems, including power modules, gate driver units, protection boards, capacitor banks, auxiliary electronics, cooling equipment, and control boards [20]. The interaction between

these elements directly affects converter efficiency, maintainability, thermal performance, manufacturing cost, and overall power density.

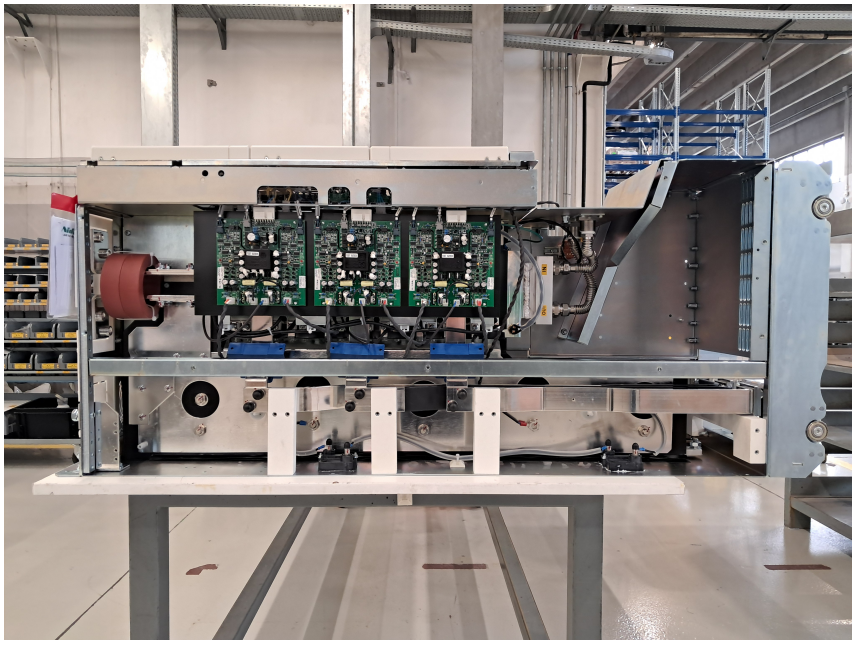

Figure 2.5: Internal layout of the Nidec AD5000 converter.

2.4.1 System Overview

The AD5000 control architecture is organized in a hierarchical structure [20]. A central control unit manages the operation of the inverter and communicates with dedicated gate driver units responsible for generating the switching signals for the power semiconductor devices.
For each inverter phase, the gate driver communicates with a protection board mounted directly on the power module. The protection board interfaces with the IGBT module and implements local protection functions, while the gate driver board performs signal conditioning and gate control.
The signal path can be summarized as:

Central Controller → Gate Driver Unit → Protection Board → IGBT Module

This architecture provides a robust and modular solution, allowing each subsystem to be independently developed and maintained. However, the presence of multiple dedicated boards increases the overall system complexity and contributes to both volume occupation and manufacturing costs.

2.4.2 Gate Driver and Protection Architecture

The current AD5000 platform employs two separate electronic boards for each phase [20]. The TPIL46CA board performs the gate driving function, while a

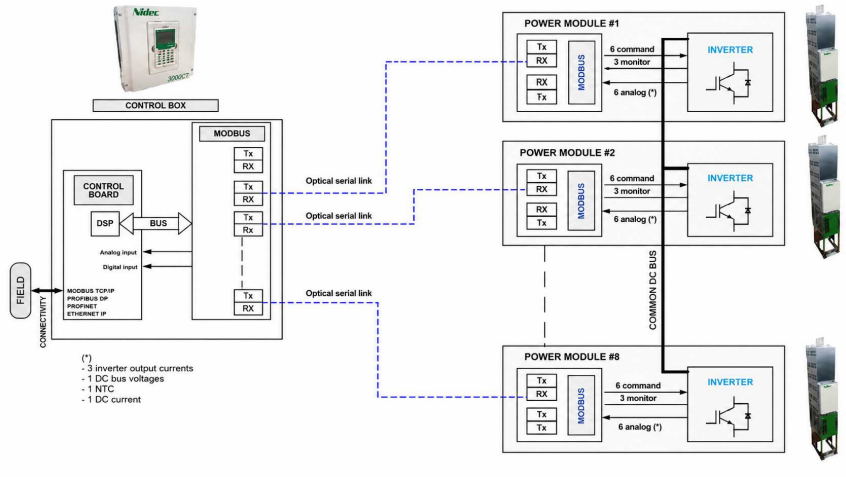

Figure 2.6: Simplified internal signal path of the AD5000 power stage.

dedicated GPG3A board is mounted directly on the power module to implement protection functions and gate resistance management.
The protection board is necessary to ensure safe operation of the semiconductor devices by monitoring abnormal operating conditions and implementing fast protection mechanisms. In addition, it provides the interface required to manage the gate resistance network used during turn-on and turn-off transitions.
Although this architecture has proven to be reliable in industrial operation, it introduces additional components, interconnections, wiring, and assembly operations. As a consequence, both the occupied volume and the manufacturing cost increase.
Future developments aim to integrate the gate driver and protection functions into a single electronic unit directly associated with the power module. Such an approach would simplify the overall architecture, reduce the number of electronic boards, and improve converter compactness.

2.4.3 Mechanical Layout and Power Density Considerations

During the industrial analysis conducted throughout this work, particular attention was devoted to the physical layout of the current AD5000 platform.
The liquid-cooled implementation currently adopted by Nidec originates from a previously developed air-cooled platform. In order to minimize redesign effort and accelerate industrialization, several mechanical elements of the original architecture were retained.
As a consequence, the present converter contains a significant amount of unused internal volume, as visible in Figure 2.5. The power conversion stage

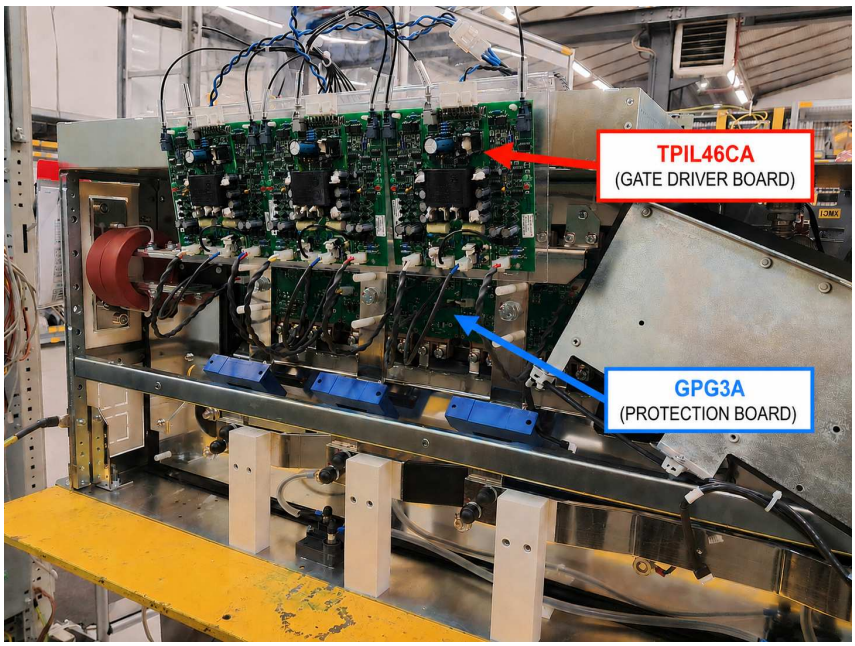

Figure 2.7: Gate driver and protection boards adopted in the present AD5000 architecture.

occupies only a fraction of the available space, while several areas remain partially unutilized due to legacy mechanical constraints inherited from the previous platform.
A detailed inspection of the converter reveals that the auxiliary section, including the cooling system, control electronics, and support equipment, occupies a relatively fixed volume within the cabinet. Therefore, future reductions in cabinet dimensions cannot be achieved by modifying the auxiliary section, but rather through optimization of the power conversion stage itself.
The current drive units have an approximate width of 290 mm. The development target for the next-generation platform is a reduction to approximately 240 mm per drive.
Considering the required side clearances for installation and maintenance, this reduction would enable:

- Two drives to be integrated within a 600 mm cabinet;
- Three drives to be integrated within an 800 mm cabinet.

For comparison, the current solution requires approximately 1000 mm of cabinet width to accommodate three drives, as we can see in Figure 2.4 .
The reduction in converter dimensions would significantly increase power density while preserving the functionality of the existing auxiliary systems. Consequently, the adoption of more compact semiconductor modules and a simplified gate driver architecture represents one of the most promising development paths for future generations of the AD5000 platform.

2.5 Thesis Objectives

The main objective of this thesis is the evaluation of possible improvements to the existing Nidec AD5000 inverter platform through the adoption of modern power semiconductor technologies and a more compact converter architecture. The study is motivated by the increasing demand for higher power density, improved performance, and reduced system cost in marine propulsion applications. Particular attention is devoted to the impact of semiconductor technology on converter dimensions, thermal behaviour, and overall system architecture.
Based on the observations collected during the internship activities, three primary objectives were identified: reduction of system size, performance improvement, and cost reduction.

2.6 Possible Improvement Strategies

Several technological solutions can be considered to improve the performance of modern marine inverter systems.
The continuous evolution of power semiconductor devices has introduced new opportunities for increasing switching frequency, reducing losses, and improving converter power density.
Among the most promising approaches are the adoption of new-generation IGBTs and the integration of wide-bandgap semiconductor technologies such as Silicon Carbide MOSFETs [5, 11].

2.6.1 New Generation IGBTs

Modern power converters are required to deliver higher output power while maintaining compact dimensions, reduced cooling requirements, and high efficiency. As a result, improving power density has become one of the main objectives of semiconductor manufacturers.
Unlike earlier generations, where the primary focus was reducing switching losses, modern IGBT development aims to simultaneously improve electrical performance, thermal behaviour, and current handling capability. Studies have shown that, in high-power converter applications, conduction losses often remain the dominant contribution to the total semiconductor losses. Consequently, reducing the on-state voltage drop of both the IGBT and the freewheeling diode continues to be a key design target.
To achieve these objectives, manufacturers have introduced several structural innovations at chip level. Advanced trench gate architectures and optimized

carrier distribution techniques allow a reduction of both conduction and switching losses while maintaining safe operating conditions. In addition, modern device structures improve switching behaviour by reducing voltage overshoots and oscillations during turn-off transients, enabling higher switching speeds and improved reliability.

Another important aspect of new-generation IGBTs is the improvement of thermal performance. By increasing the effective chip area and optimizing the internal package structure, manufacturers are able to reduce the junction-to-case thermal resistance. Lower thermal resistance allows more efficient heat dissipation, resulting in lower junction temperatures for the same operating conditions or, alternatively, higher current capability without increasing the device temperature.

The combined reduction of electrical losses and thermal resistance enables significant improvements in power density. Recent studies report output power increases of approximately 25% while maintaining the same package platform, demonstrating the potential of new-generation IGBT technologies for future high-power converter applications [11].

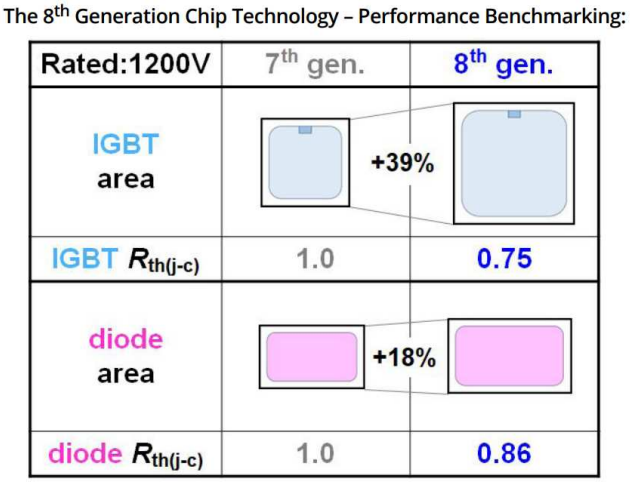

Figure 2.8: Power density improvement enabled by new-generation IGBT technology.

2.6.2 SiC MOSFET Technology

Silicon Carbide (SiC) MOSFETs represent one of the most significant advancements in modern power semiconductor technology [5, 7]. As a wide-bandgap (WBG) device, the SiC MOSFET offers superior electrical and thermal properties compared to conventional silicon-based power devices, making it particularly attractive for high-efficiency power conversion systems.

The main advantage of SiC technology originates from the material properties of silicon carbide itself. Compared to silicon, SiC exhibits a larger bandgap,

higher critical electric field, higher thermal conductivity, and higher electron saturation velocity. These characteristics allow the realization of devices capable of operating at higher voltages, higher temperatures, and significantly higher switching frequencies.

One of the most important benefits of SiC MOSFETs is the substantial reduction of switching losses. Unlike IGBTs, SiC MOSFETs do not exhibit minority-carrier storage effects and therefore do not suffer from the current-tail phenomenon during turn-off. As a result, switching transitions are significantly faster and the energy dissipated during commutation is greatly reduced.

The reduction of switching losses allows operation at considerably higher switching frequencies. Higher switching frequency enables the use of smaller passive components such as filters, inductors, and transformers, contributing to a reduction in the overall size and weight of the converter. This improvement directly translates into increased power density, which is one of the main design targets of modern power electronic systems.

In addition to their superior dynamic performance, SiC MOSFETs also exhibit lower conduction losses, particularly at elevated temperatures. The lower on-state resistance and improved thermal properties of the material contribute to higher overall efficiency and reduced cooling requirements. Several studies have reported converter efficiencies exceeding 98% and power densities above 70 kW/L when SiC devices are employed in high-performance inverter applications.

The combination of high efficiency, reduced cooling requirements, compact passive components, and increased switching frequency makes SiC MOSFETs particularly attractive for electric vehicles, renewable energy systems, aerospace applications, fast charging infrastructure, and future high-power industrial drives. For these reasons, SiC technology is widely regarded as one of the most promising candidates for the next generation of power converters.

2.6.3 Challenges and Limitations of SiC MOSFETs

Despite their outstanding performance, SiC MOSFETs still present several challenges that currently limit their widespread adoption in many industrial applications [7].

One of the primary concerns is the higher device cost compared to conventional silicon IGBTs. The manufacturing process of silicon carbide devices is more complex and requires specialized materials and fabrication techniques, resulting in significantly higher production costs. Although the efficiency improvements can compensate for the increased device price in some applications, the economic impact remains an important consideration.

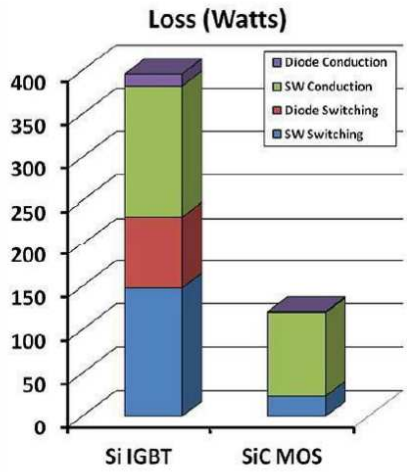

Figure 2.9: Comparison between conventional IGBT and SiC MOSFET switching losses.

Another challenge is related to the extremely fast switching speed of SiC MOSFETs. While high switching speed reduces switching losses, it also generates very high dv/dt and di/dt values. These rapid transients can lead to increased electromagnetic interference (EMI), voltage overshoots, ringing phenomena, and higher sensitivity to parasitic inductances and capacitances within the converter layout. Consequently, PCB design, busbar layout, and gate driver implementation become significantly more critical than in traditional IGBT-based systems. In motor-drive applications, high switching frequencies and steep voltage gradients may also increase the electrical stress applied to motor insulation systems, especially when long cables are used between the inverter and the machine. The combination of cable reflections and high dv/dt pulses can produce overvoltages at the motor terminals and may contribute to partial discharge phenomena if the insulation system is not properly designed. This aspect is particularly relevant in large industrial and marine drives, where reliability and lifetime requirements are stringent.

The gate oxide reliability of SiC MOSFETs has also been extensively investigated [7]. Long-term electrical stress may cause threshold voltage shifts and gate oxide degradation, potentially affecting device performance and reliability. Although substantial improvements have been achieved in recent generations, reliability remains an active research topic.

Short-circuit robustness represents another important limitation [7]. Compared to IGBTs, SiC MOSFETs generally exhibit lower short-circuit withstand capability due to their high current density and fast switching behaviour. Consequently, protection systems must be capable of detecting and interrupting fault conditions within a few microseconds to prevent device failure.

Thermal management can also present additional challenges. Although SiC

devices are capable of operating at higher junction temperatures, their smaller chip area often results in higher power density within the semiconductor package. This requires careful thermal design to fully exploit the advantages offered by the technology.
Therefore, while SiC MOSFETs offer significant advantages in terms of efficiency, switching performance, and power density, their implementation requires careful consideration of cost, reliability, electromagnetic compatibility, and protection requirements. For this reason, IGBT technology remains the preferred solution in many medium- and high-power industrial applications, while SiC devices are increasingly adopted in applications where maximum efficiency and power density are the primary design objectives.

2.6.4 Integrated Gate Driver Concept

Besides the introduction of more compact power modules, further improvements can be achieved through the integration of gate driver and protection functions.
Modern power electronic systems are increasingly moving towards highly integrated solutions, where auxiliary electronics are mounted directly on the power module [4, 11]. This approach reduces wiring complexity, minimizes parasitic inductances, simplifies assembly procedures, and contributes to a more compact converter architecture.
An example of this concept is shown in Fig. 2.10, where the gate driver unit is directly integrated with an LV100 power module.

Figure 2.10: Example of an integrated gate driver unit directly mounted on an LV100 power module.

Compared to conventional architectures based on multiple independent boards, integrated solutions reduce the number of interconnections required by the power stage and enable a more efficient utilization of the available cabinet

volume. Furthermore, the shorter electrical paths between the gate driver and the semiconductor devices improve switching control and reduce sensitivity to parasitic effects.

However, the increased integration also introduces new design challenges. The gate driver electronics operate in close proximity to the power semiconductor devices and are therefore exposed to higher temperatures, stronger electromagnetic disturbances, and more demanding insulation requirements. Consequently, particular attention must be devoted to thermal management, electromagnetic compatibility, and long-term reliability.

Despite these challenges, the integration of gate driver and protection functions is widely regarded as a key enabling technology for future high-power converters, as it supports the continuous increase of power density while simplifying the overall system architecture.

Chapter 3

Simulation Model

3.1 Modelling Approach

This chapter presents the electro-thermal simulation framework developed to evaluate and compare different IGBT technologies for marine propulsion inverter applications. The model is implemented in MATLAB and combines electrical loss calculations with a dynamic thermal network in order to estimate power dissipation, junction temperature evolution, and converter efficiency.
The framework is based on manufacturer datasheet information and allows direct comparison between different semiconductor technologies under identical operating conditions.
Three Infineon power modules are considered:

- FS450R17OE4 (reference device) [8]
- FF1200XTR17T2P5 (new-generation device) [9]
- FF1400R17T2P8 (future-generation device) [10]

The FS450R17OE4 represents the current solution adopted in the investigated converter platform. Since a single module cannot withstand the required current level, three devices are connected in parallel.
The FF1200XTR17T2P5 represents a more recent IGBT technology with sufficient current capability to eliminate the need for parallelization.
The FF1400R17T2P8 is considered as a representative example of future high-current IGBT technologies and is included to evaluate the potential benefits achievable through further semiconductor developments.
The simulation framework has been designed to allow rapid switching between devices while automatically loading the corresponding electrical, switching, and thermal parameters.

3.2 Electrical Model and Switching Logic

The phase current is modeled as a sinusoidal waveform with fixed amplitude and phase shift:

$$i(t) = \sqrt{2} I_{\mathrm{RMS}} \cos\left(2\pi f t - \varphi\right) \tag{3.1}$$

The line-to-line RMS output voltage is given by:

$$V_{\mathrm{ac}} = \frac{\sqrt{3}}{\sqrt{2}} m_a \frac{V_{\mathrm{dc}}}{2} \tag{3.2}$$

The total output power delivered to the load is:

$$P_{\mathrm{load}} = \sqrt{3} V_{\mathrm{ac}} I_{\mathrm{RMS}} \cos\varphi \tag{3.3}$$

The inverter leg is controlled using Sinusoidal Pulse Width Modulation (SPWM), which is one of the most widely adopted modulation techniques in industrial voltage source inverters [2].
In SPWM, a low-frequency sinusoidal reference waveform is compared against a high-frequency triangular carrier signal. The reference signal is defined as:

$$v_{\sin}(t) = m_a \cos(2\pi f t) \tag{3.4}$$

where m_a is the modulation index and f is the fundamental output frequency. The carrier signal is a symmetric triangular waveform at switching frequency f_s.
The switching state of the inverter leg is determined by the comparison:

$$s(t) = \begin{cases} 1 & \text{if } v_{\sin}(t) \geq v_{\mathrm{tri}}(t) \\ 0 & \text{otherwise} \end{cases} \tag{3.5}$$

When $s(t) = 1$, the high-side IGBT is commanded ON and the phase voltage is approximately $+V_{\mathrm{dc}}/2$. Conversely, when $s(t) = 0$, the low-side IGBT is ON and the phase voltage is approximately $-V_{\mathrm{dc}}/2$.
Depending on the instantaneous sign of the phase current, current conduction is naturally transferred between IGBTs and free-wheeling diodes. This results in four distinct operating quadrants, each associated with a specific conducting device (Q1, D1, Q2, or D2) as shown in figure 3.1.
Switching losses are generated only during state transitions of $s(t)$ and are evaluated by detecting changes between consecutive switching states.

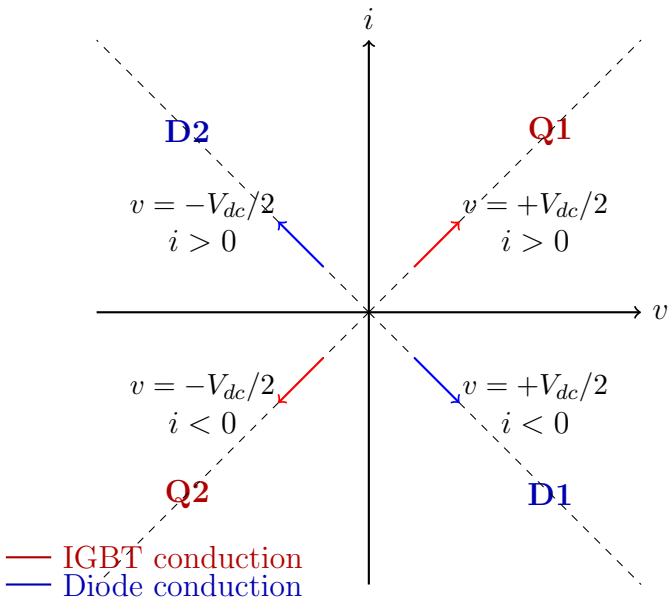

Figure 3.1: Four-quadrant conduction map of a single inverter leg with current direction.

3.3 Time-Step Selection and Switching Event Resolution

The accuracy of the proposed electro-thermal simulation strongly depends on the choice of the simulation time-step T_{step}. In particular, special care must be taken to correctly resolve switching events introduced by the SPWM modulation.

3.3.1 Switching Event Loss of Resolution

During the initial development phase, incorrect loss and temperature results were observed when increasing the switching frequency from 2 kHz to 4 kHz while keeping the same simulation time-step. A detailed analysis revealed that some switching events were being missed by the simulation.
This issue arises when the simulation time-step becomes too large with respect to the switching period $T_s = 1/f_s$. If T_{step} is not sufficiently small, the PWM carrier and reference signals may change state between two consecutive simulation samples, causing:

- missed turn-on or turn-off events,
- incorrect switching energy accumulation,
- underestimation or overestimation of switching losses,
- non-physical temperature evolution.

Since switching losses are evaluated only at detected commutation instants, missing even a small fraction of transitions leads to large errors in both electrical and thermal results.

3.3.2 Time-Step Scaling with Switching Frequency

To ensure correct detection of all switching events, the simulation time-step must be chosen significantly smaller than the switching period. In this work, it was observed that doubling the switching frequency from 2 kHz to 4 kHz required halving the simulation time-step to maintain numerical accuracy.
This choice guarantees that:

- all PWM commutations are correctly resolved,
- switching energies are evaluated at the correct instants,
- conduction intervals are properly identified,
- the thermal power profile remains physically consistent.

The adopted time-step therefore scales inversely with the switching frequency:

$$T_{\text{step}} \propto \frac{1}{f_s} \tag{3.6}$$

3.3.3 Impact on Loss and Thermal Estimation

Failing to resolve switching events leads to erroneous loss calculation, which directly propagates into the thermal model. Since the junction temperature depends on the accumulated power dissipation, missed commutations can result in:

- artificially low switching losses,
- underestimated average junction temperature,
- misleading conclusions on device suitability.

For this reason, a sufficiently small simulation time-step is a fundamental requirement for reliable electro-thermal analysis, particularly when comparing different switching frequencies or semiconductor technologies.

3.4 Loss Model Based on Infineon Data

The accuracy of the proposed simulation framework strongly depends on the correct estimation of semiconductor power losses. Instead of relying on simplified analytical models, the developed approach directly exploits the characterization data provided by Infineon in the device datasheets [8, 9, 10].
Both conduction and switching losses are evaluated using numerical lookup tables derived from the manufacturer curves. This methodology allows the model to reproduce the actual behaviour of the devices while maintaining a reasonable computational complexity.

3.4.1 Datasheet Data Extraction

The electrical characteristics required for the simulation are provided by Infineon in graphical form. These include switching energy curves, conduction characteristics, and gate resistance correction factors.
The original datasheet plots were digitized and converted into numerical lookup tables suitable for MATLAB implementation. The resulting tables preserve the dependence of the electrical quantities on current, temperature, gate resistance, and operating voltage.
The extracted data constitute the foundation of the entire loss calculation procedure. By directly using manufacturer characterization data, the simulation model remains closely linked to the real device behaviour and avoids the inaccuracies often associated with simplified theoretical approximations.

3.4.2 Switching Losses

Switching losses are evaluated at every commutation event detected by the PWM algorithm. Turn-on energy (E_{on}), turn-off energy (E_{off}), and reverse recovery energy (E_{rec}) are obtained through interpolation of the extracted lookup tables.
The switching energies depend on several operating parameters:

- collector current,
- junction temperature,
- DC-link voltage,
- gate resistance.

For each switching event, the simulation first determines the instantaneous current flowing through the device and its junction temperature. The corre-

sponding switching energy is then obtained through interpolation of the manufacturer data.
The general dependency can be expressed as:

$$E_{sw} = f(I_C, T_j, R_g, V_{DC})$$

where I_C is the collector current, T_j is the junction temperature, R_g is the gate resistance, and V_{DC} is the DC bus voltage.
The switching energy increases significantly with current and temperature. This behaviour is particularly evident at high current levels, where switching losses become one of the dominant contributions to the total inverter losses.

3.4.3 Current and Temperature Interpolation

The manufacturer provides switching energy data only for a limited number of temperatures and current values. During simulation, however, the operating conditions continuously vary.
To overcome this limitation, a two-stage interpolation procedure is implemented. The switching energy is first interpolated with respect to current for each available temperature curve. Subsequently, a second interpolation is performed across temperature to obtain the final switching energy corresponding to the actual junction temperature.
This approach allows smooth transitions between operating points and guarantees continuity of the calculated losses.

3.4.4 Gate Resistance Dependence

The switching behaviour of an IGBT is strongly influenced by the external gate resistance. Increasing the gate resistance reduces the switching speed, leading to lower voltage and current slopes but higher switching energies.
For the FF1200XTR17T2P5 device, Infineon provides dedicated correction tables that describe the variation of switching energies as a function of gate resistance and temperature [9].
The simulation uses these correction coefficients to accurately adapt the switching energy values to the selected gate resistance.
The gate resistance therefore represents an important design parameter, since it directly affects the trade-off between switching losses, electromagnetic interference, and voltage overshoots.

3.4.5 DC-Link Voltage Scaling

Datasheet switching energies are usually specified for a reference DC-link voltage. In practical applications, the operating voltage may differ from the reference condition.
To account for this effect, the switching energies are scaled according to:

$$k_V = \frac{V_{DC}}{V_{ref}}$$

where V_{ref} is the voltage used by the manufacturer during characterization.
The final switching energy is therefore calculated as:

$$E_{sw} = E_{datasheet} \cdot k_R \cdot k_V$$

where k_R represents the gate resistance correction factor.
This correction allows the model to remain valid under different operating voltages without requiring additional manufacturer data. This scaling assumes an approximately linear dependence of switching energy on DC-link voltage, which is a commonly adopted approximation when detailed voltage-dependent characterization data are not available [13]. The approach provides a practical method for adapting the datasheet values to the operating conditions considered in the simulation.

3.4.6 Conduction Losses

Conduction losses are evaluated using manufacturer datasheet characteristics for both the IGBT and the freewheeling diode [8, 9, 10]. The original datasheet curves were digitized and converted into numerical lookup tables, allowing the voltage drop across each device to be determined as a function of current and junction temperature.
For the IGBT, the on-state collector-emitter voltage is obtained through interpolation of the extracted lookup tables:

$$V_{CE} = f(I_C, T_j)$$

where I_C is the collector current and T_j is the junction temperature.
The conduction energy dissipated during each simulation step is then calculated as:

$$E_{cond} = V_{CE}(I_C, T_j) \cdot I_C \cdot T_{step}$$

where T_{step} is the simulation time step.

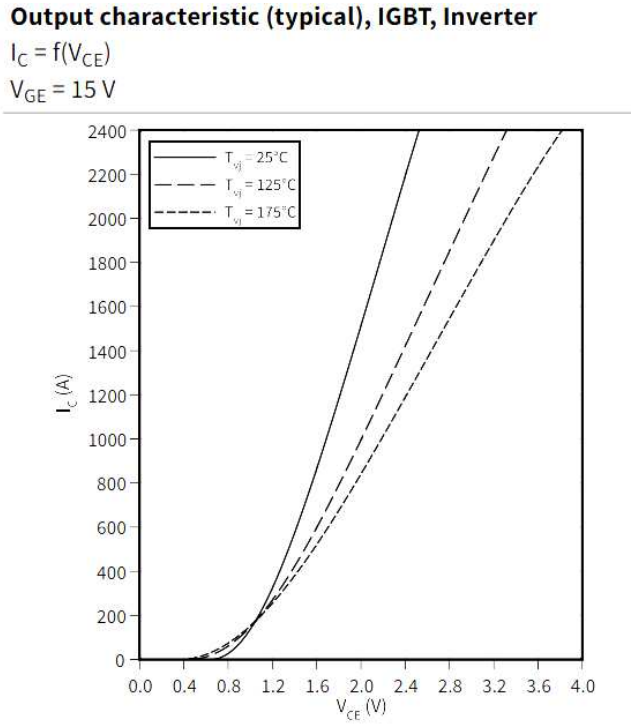

Figure 3.2: Output characteristics of the FF1200XTR17T2P5 IGBT at different junction temperatures, digitized from the manufacturer datasheet and converted into numerical lookup tables used to estimate the collector-emitter voltage drop during conduction [9].

As shown in Fig. 3.2, the collector-emitter voltage depends on both the collector current and the junction temperature. The extracted curves are used to generate the lookup tables employed by the conduction loss model.
The same methodology is applied to the freewheeling diode. The forward voltage drop is obtained from the manufacturer forward characteristic and interpolated as a function of diode current and junction temperature:

$$V_F = f(I_F, T_j)$$

The corresponding conduction energy is calculated according to:

$$E_{cond,D} = V_F(I_F, T_j) \cdot I_F \cdot T_{step}$$

Fig. 3.3 shows the forward voltage characteristics of the freewheeling diode. Similar to the IGBT model, the voltage drop is obtained through interpolation as a function of current and junction temperature.
It can be observed that both the IGBT collector-emitter voltage and the diode forward voltage exhibit a significant dependence on junction temperature. Consequently, the use of temperature-dependent lookup tables is essential to accurately reproduce the electro-thermal behaviour of the power module.
This approach allows the temperature dependence of both the IGBT and diode

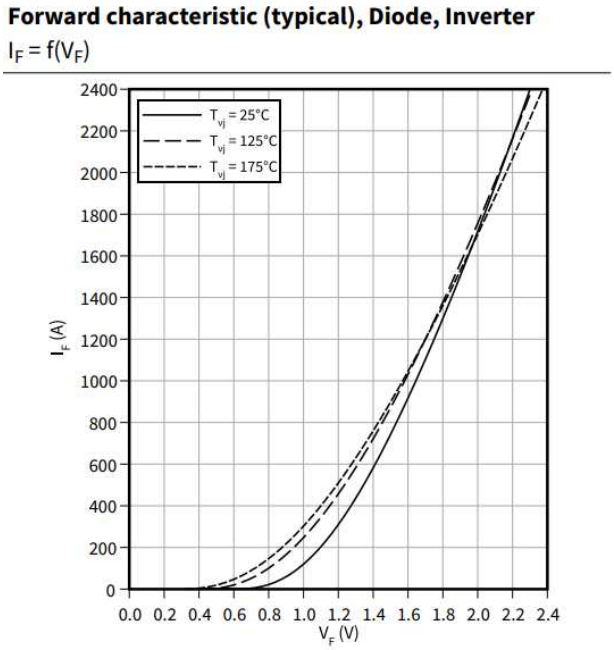

Figure 3.3: Forward voltage characteristics of the FF1200XTR17T2P5 freewheeling diode at different junction temperatures, digitized from the manufacturer datasheet and used to calculate diode conduction losses through interpolation of the forward voltage drop [9].

voltage drops to be accurately represented throughout the simulation, improving the accuracy of the electro-thermal model.

3.4.7 Interpolation Structure

The complete loss calculation procedure can be summarized by the workflow shown in Figure 3.4.
Starting from the manufacturer datasheet curves, the information is converted into numerical lookup tables. During simulation, the instantaneous operating conditions are used to interpolate the corresponding electrical characteristics and calculate the associated losses.

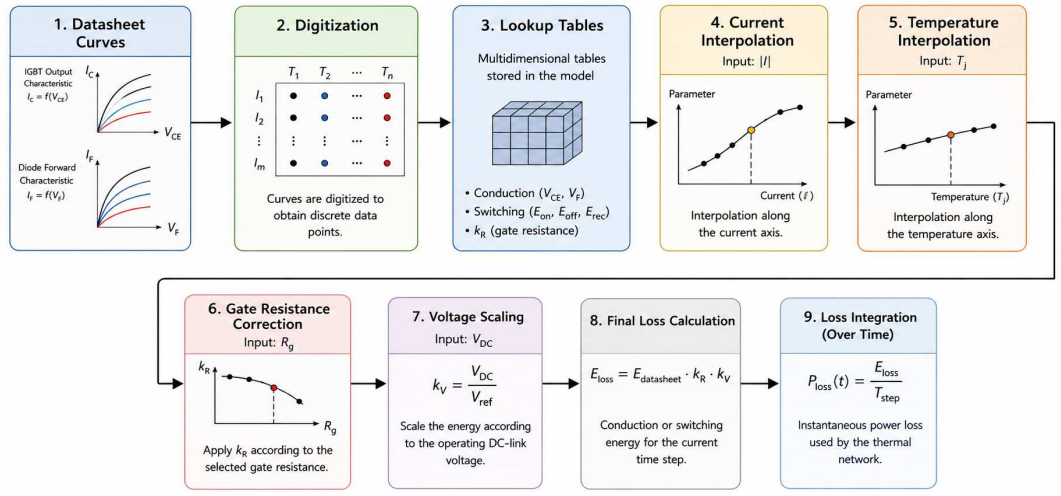

Figure 3.4: Workflow adopted for datasheet data extraction, lookup-table generation and loss calculation.

This methodology allows the simulation model to accurately reproduce the behaviour of the investigated semiconductor devices while preserving flexibility and computational efficiency.

3.5 Thermal Model

Each semiconductor device (IGBT or diode) is modeled using a Foster-type thermal RC network, as introduced in Section 1.4.4 [12]. The thermal path from the silicon junction to the ambient is divided into two main parts:

- a **junction-to-case** dynamic thermal impedance, modeled by a multi-stage RC network;
- a **case-to-heatsink** static thermal resistance.

This approach allows accurate modeling of both the transient and steady-state thermal behavior while maintaining low computational complexity.

3.5.1 Junction-to-Case Thermal Model

The junction-to-case thermal behavior of each device is represented by a Foster RC network, whose parameters are provided in the manufacturer datasheet in terms of thermal resistance R_{th} and thermal time constant τ . The corresponding thermal capacitance is obtained as:

$$C_{\text{th}} = \frac{\tau}{R_{\text{th}}} \tag{3.7}$$

For each RC stage, the temperature rise ΔT_{jc} is governed by the first-order differential equation:

$$\frac{d\Delta T_{\text{jc}}}{dt} = \frac{P(t) - \Delta T_{\text{jc}}/R_{\text{th}}}{C_{\text{th}}} \tag{3.8}$$

where $P(t)$ is the instantaneous power dissipated by the device.

3.5.2 Discrete-Time Implementation

To enable time-domain simulation, the thermal differential equation is discretized using a forward Euler method with a simulation time-step T_{step}. The resulting update equation is:

$$\Delta T_{\text{jc}}(k+1) = \Delta T_{\text{jc}}(k) + \left(P(k) - \frac{\Delta T_{\text{jc}}(k)}{R_{\text{th}}} \right) \frac{T_{\text{step}}}{C_{\text{th}}} \tag{3.9}$$

This formulation is applied independently to each RC branch of the Foster network and to each semiconductor device.
The numerical integration is stable and accurate due to the large separation between the electrical time-step (μs range) and the thermal time constants (ms–s range).

3.5.3 Case-to-Heatsink Thermal Path

The case-to-heatsink thermal path is modeled as a purely resistive element $R_{\text{th,CH}}$. The corresponding temperature rise is computed as:

$$\Delta T_{\text{ch}} = P_{\text{avg}} \cdot R_{\text{th,CH}} \tag{3.10}$$

where P_{avg} is a low-pass filtered version of the instantaneous power. This filtering reflects the fact that the case temperature cannot follow high-frequency power fluctuations.

3.5.4 Power Filtering for Thermal Stability

The instantaneous power dissipation exhibits large spikes due to switching events. Directly applying this power to the thermal RC model would lead to numerical artifacts and unrealistically high temperature excursions.
To address this issue, the power signal is filtered using a first-order discrete-time low-pass filter:

$$P_{\mathrm{f}}(k) = K \cdot P(k) + (1 - K) \cdot P_{\mathrm{f}}(k - 1) \tag{3.11}$$

where K is a small filtering coefficient. This operation does not alter the average dissipated power but removes non-physical high-frequency components, ensuring a realistic thermal response.

3.5.5 Total Junction Temperature

The total junction temperature is finally obtained by summing all thermal contributions:

$$T_j = T_{\mathrm{hs}} + \Delta T_{\mathrm{ch}} + \sum_{n=1}^{N} \Delta T_{\mathrm{jc},n} \tag{3.12}$$

where:

- T_{hs} is the heatsink temperature,
- ΔT_{ch} is the case-to-heatsink temperature rise,
- $\Delta T_{\mathrm{jc},n}$ are the temperature rises of the individual Foster RC stages.

This modeling approach provides an accurate and computationally efficient thermal representation suitable for long time-domain simulations involving high switching frequencies.

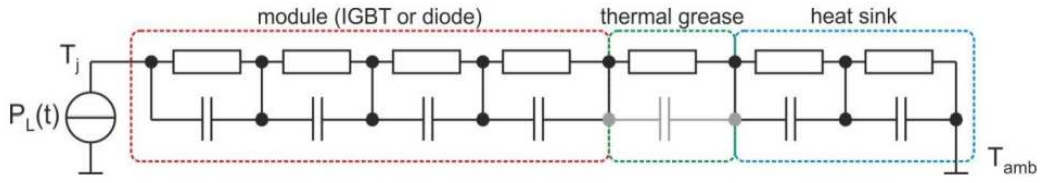

Figure 3.5: Representation of the Foster thermal model implemented in MATLAB.

3.6 Simulation Setup and Model Validation

The electro-thermal model described in the previous sections was implemented in MATLAB in order to evaluate the behaviour of different power semiconductor devices under operating conditions representative of the AD5000 converter platform.

The simulation parameters reported in Table 3.1 are derived from the AD5W740L reference configuration introduced in Fig. 2.3. This liquid-cooled inverter belongs to the 690 V_{AC} class and operates with a DC-link voltage up to approximately 1110 V_{DC}. According to the reference platform data, the nominal operating condition is characterized by a switching frequency of 2 kHz and a total output current of 680 A_{RMS} [16, 20].

These values are used as the baseline for the electro-thermal simulations and for the comparison between the currently adopted IGBT solution and the investigated new-generation modules. The main objective is to evaluate the possible improvement in terms of semiconductor losses, junction temperature, current capability and potential reduction of the power stage volume.

Table 3.1: Simulation parameters

Parameter	Value
DC-link Voltage	1110 V
Output Frequency	50 Hz
Power Factor	0.8
Modulation Index	1.0
RMS Current	680 A
Switching Frequency	2 kHz – 4 kHz
Heatsink Temperature	60 °C

Although the nominal switching frequency of the reference drive is 2 kHz, additional simulations were also performed at higher switching frequencies up to 4 kHz in order to evaluate the impact of the switching frequency on semiconductor losses and thermal behaviour.

Since the DC-link voltage can reach approximately 1110 V_{DC}, IGBT modules with a blocking voltage rating of 1700 V are required. In a two-level inverter, the steady-state DC-link voltage is not the only design constraint, since temporary overvoltages can occur during switching transients due to parasitic inductances in the commutation loop. Therefore, the 1700 V voltage class provides the necessary voltage margin for safe and reliable operation under high-power switching conditions [8, 9, 10].

The current value reported in Table 3.1 refers to the total output current of the drive. In the reference configuration based on the FS450R17OE4 module, three power modules are connected in parallel for each inverter leg. Therefore,

assuming ideal current sharing, each FS450R17OE4 module conducts approximately one third of the total current, corresponding to 226.7 A_{RMS}.
The investigated FF1200XTR17T2P5 and FF1400R17T2P8 modules are instead evaluated as possible higher-current alternatives. The objective is to assess whether the same drive current can be handled by a single module, avoiding the need for parallel-connected devices and simplifying the overall power stage architecture.
At each simulation time-step, the electro-thermal model performs the following operations:

1. determine the switching state and the conducting semiconductor device;
2. compute conduction and switching energy losses;
3. convert energy losses into instantaneous power dissipation;
4. apply low-pass filtering to obtain the thermal power input;
5. update the thermal RC network states;
6. store junction temperatures and losses for post-processing.

This coupled electro-thermal loop allows the semiconductor losses to depend on the instantaneous junction temperature, while the junction temperature is itself updated according to the dissipated power. In this way, the mutual interaction between electrical and thermal phenomena is reproduced throughout the complete inverter operation.
Before performing the comparative analysis, the MATLAB implementation was validated through comparison with Infineon IPOSIM simulations. IPOSIM is a PLECS-based simulation environment provided by Infineon for the estimation of semiconductor losses and thermal behaviour under user-defined operating conditions [14, 15].
Identical operating conditions were applied in both environments, and the resulting conduction losses, switching losses, total semiconductor losses and junction temperatures were compared.
The validation was performed using the FS450R17OE4 module at a DC-link voltage of 1110 V, an output current of 226.7 A_{RMS} per module, a switching frequency of 4 kHz, an output frequency of 50 Hz and a power factor equal to 0.8.
The validation results show good agreement between the proposed MATLAB model and the reference simulations obtained from Infineon IPOSIM. For most of the investigated quantities, the deviation remains below 1%, while the maximum observed difference is 2.87% for the diode conduction losses.

Table 3.2: MATLAB model validation against Infineon IPOSIM

Quantity	MATLAB	IPOSIM	Error (%)
Q1 $T_{j,max}$ [°C]	116.7	118.06	1.15
Q1 P_{cond} [W]	144.9	146.0	0.75
Q1 P_{sw} [W]	336.0	338.6	0.77
Q1 P_{tot} [W]	480.9	484.6	0.76
D1 $T_{j,max}$ [°C]	88.5	89.24	0.83
D1 P_{cond} [W]	26.5	25.76	2.87
D1 P_{sw} [W]	130.6	131.8	0.91
D1 P_{tot} [W]	157.1	157.56	0.29

These discrepancies are considered acceptable for engineering applications and can be attributed to differences in numerical implementation, interpolation methods and thermal network discretization between the two simulation environments. Overall, the results confirm the accuracy of the developed electro-thermal model and validate the adopted interpolation procedures. The MATLAB implementation can therefore be used for the comparative evaluation of the alternative semiconductor technologies presented in the following sections.

3.7 Simulation Results and Device Comparison

The comparative analysis initially included both the FF1200XTR17T2P5 and FF1400R17T2P8 modules.

At the beginning of the internship activities, the FF1200XTR17T2P5 represented the most suitable candidate for replacing the existing FS450R17OE4 solution. The main objective was to investigate whether a higher-current module could eliminate the need for parallel-connected devices while maintaining comparable electrical and thermal performance.

During the course of the project, Infineon introduced the FF1400R17T2P8 module, representing a newer semiconductor generation that was still in the prototyping phase at the time of the initial investigations.

Preliminary simulations showed that the FF1200XTR17T2P5 provided only limited advantages compared to the reference solution. In some operating conditions, the expected improvements were not sufficiently significant to justify a major architectural redesign. Consequently, the focus of the analysis progressively shifted towards the FF1400R17T2P8 module, which exhibited more promising characteristics in terms of power density and loss reduction.

For this reason, the following sections primarily focus on the comparison between the currently adopted FS450R17OE4 module and the FF1400R17T2P8

device.
In addition to the electrical and thermal performance, the mechanical dimensions of the investigated packages represent an important aspect for the power density evaluation. The currently adopted FS450R17OE4 EconoPACK+ module has approximate dimensions of 162 mm × 150 mm, while the LV100 package considered for the new-generation solution has dimensions of approximately 100 mm × 140 mm × 40 mm.
Therefore, the adoption of the LV100 package allows a significant reduction of the module footprint. This aspect is particularly relevant for the development of a more compact power stage, especially when combined with the possibility of replacing parallel-connected devices with a single higher-current module [8, 11].

3.7.1 Comparison at Nominal Operating Conditions

The first comparison was performed at the nominal operating point of the converter, corresponding to a DC-link voltage of 1110 V, output current of 680 Arms, output frequency of 50 Hz, power factor of 0.8 and switching frequencies ranging from 2 kHz to 4 kHz.
The obtained results are summarized in Table 3.3.

Table 3.3: Total semiconductor losses per inverter leg at 680 Arms

f_{sw}	FS450R17OE4 [W]	FF1400R17T2P8 [W]	Reduction [%]
2 kHz	2303.7	1991.9	13.54
3 kHz	2942.7	2528.9	14.06
4 kHz	3824.1	3268.3	14.53

The results show that the FF1400R17T2P8 module consistently achieves lower semiconductor losses than the reference FS450R17OE4 solution. Depending on the switching frequency, the reduction ranges from approximately 13.5

3.7.2 Thermal Behaviour

The corresponding junction temperatures were evaluated using the electro-thermal model described in the previous sections.
Values in parentheses indicate the maximum junction temperature.
The results indicate that the FF1400R17T2P8 module operates at slightly higher junction temperatures than the reference solution.
This behaviour may initially appear counterintuitive considering the reduction in total losses. However, the new-generation module is characterized by a

Table 3.4: Mean junction temperature comparison at 680 Arms

f_{sw}	FS450R17OE4 [°C]	FF1400R17T2P8 [°C]
2 kHz	89.8 (96.4)	92.8 (96.7)
3 kHz	97.5 (106.8)	101.9 (106.6)
4 kHz	108.2 (118.1)	114.3 (120.6)

significantly more compact package structure and therefore exhibits a reduced heat exchange area and a higher thermal resistance.
Consequently, lower losses do not necessarily translate into lower junction temperatures. Despite the observed temperature increase, all operating conditions remain well below the maximum allowable junction temperature of the device.

3.7.3 Operation at Increased Current Levels

In order to evaluate the available performance margin offered by the new semiconductor technology, additional simulations were performed at an increased output current of 800 Arms.
The same operating conditions were maintained while only the output current was modified.

Table 3.5: Total semiconductor losses per inverter leg at 800 Arms

f_{sw}	FS450R17OE4 [W]	FF1400R17T2P8 [W]	Reduction [%]
2 kHz	2785.2	2418.6	13.16
3 kHz	3544.5	3067.6	13.46
4 kHz	4609.5	3968.8	13.90

Even at the higher current level, the FF1400R17T2P8 module continues to exhibit lower total losses than the reference solution, confirming the advantages of the newer technology under demanding operating conditions.

Table 3.6: Mean junction temperature comparison at 800 Arms

f_{sw}	FS450R17OE4 [°C]	FF1400R17T2P8 [°C]
2 kHz	96.4 (103.1)	100.1 (105.1)
3 kHz	105.8 (114.1)	111.1 (117.4)
4 kHz	119.4 (129.6)	126.5 (134.3)

Values in parentheses indicate the maximum junction temperature.

3.7.4 Discussion of Results

The comparison demonstrates that the adoption of new-generation IGBT modules provides benefits that extend beyond a simple reduction of semiconductor losses.

The FF1400R17T2P8 module consistently achieves lower total losses than the reference FS450R17OE4 solution while maintaining acceptable operating temperatures. At the same time, the device offers higher current capability and a more compact package structure.

An additional consideration concerns the use of parallel-connected modules. The FS450R17OE4 solution requires current sharing between multiple devices, whereas the FF1400R17T2P8 can operate as a single high-current module. In practical applications, perfect current sharing between parallel devices cannot always be guaranteed, potentially leading to uneven thermal stress and additional losses that are difficult to accurately represent in simulation models.

A particularly relevant result is shown in Figure 3.6. The figure compares the total semiconductor losses obtained with the reference FS450R17OE4 operating at the nominal current of 680 Arms and the FF1400R17T2P8 operating at an increased current of 800 Arms.

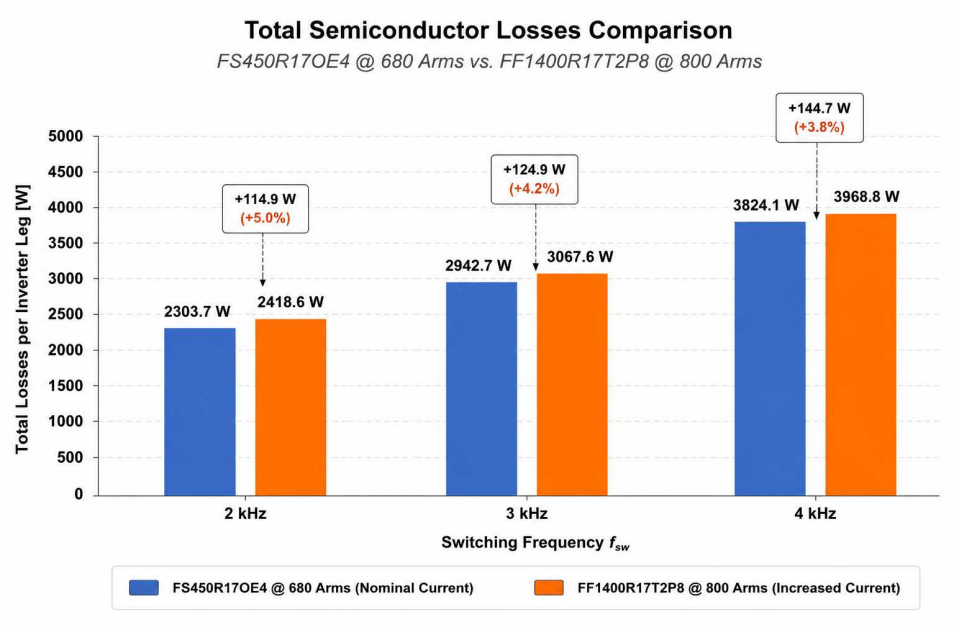

Figure 3.6: Comparison of total semiconductor losses between the FS450R17OE4 operating at 680 Arms and the FF1400R17T2P8 operating at 800 Arms.

Despite the significantly higher output current, the FF1400R17T2P8 exhibits total semiconductor losses that remain remarkably close to those of the reference solution. The increase in losses remains below 5% across the entire switching frequency range, while the output current capability is increased by

approximately 18%.

This result highlights one of the main advantages of the new-generation technology. Rather than using the improved device characteristics solely to reduce losses, the available performance margin can be exploited to increase the converter current capability and consequently the achievable power density.

Overall, the results suggest that modern high-current IGBT modules may provide an effective pathway towards higher converter power density, reduced system complexity, and improved utilization of the available installation volume. These aspects are further discussed in the following chapters together with their impact on converter dimensions and system cost.

Chapter 4

Experimental Validation

4.1 Experimental Setup

Figure 4.1 illustrates the experimental setup adopted for the switching characterization of the FS450R17OE4 modules. The test bench is composed of a high-voltage DC source, a dedicated interface board, a pulse generator, and a gate driver stage based on the TPIL40A and GPG3A driver boards [20]. The gate network was configured according to the recommendations provided for each device, allowing independent adjustment of turn-on and turn-off gate resistances.

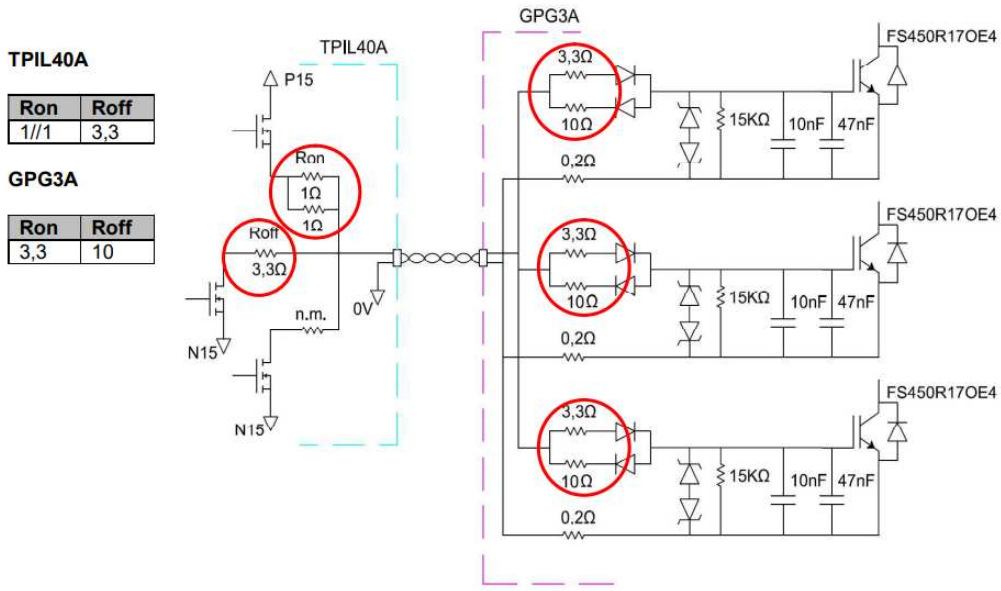

Figure 4.1: Experimental test bench used for the double-pulse characterization of the FS450R17OE4 module.

As shown in Figure 4.2, two different configurations were employed to perform double-pulse tests on both the upper and lower switch of the half-bridge leg. The switching waveforms were acquired by measuring the collector-emitter

voltage VCE, gate command signals, and load current through a Rogowski probe.

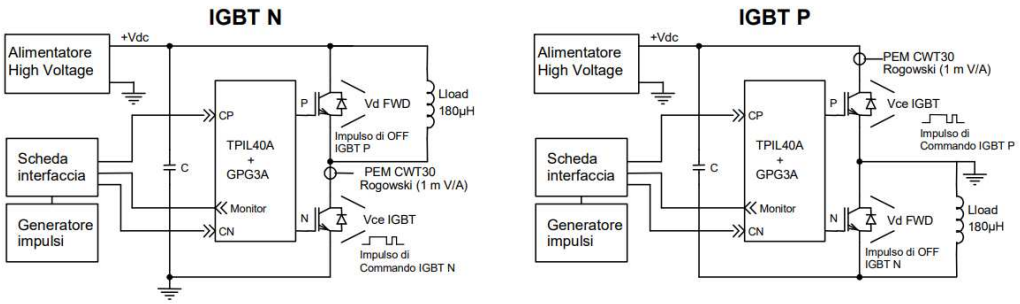

Figure 4.2: Double-pulse test configurations adopted for the characterization of the upper and lower switches.

4.1.1 Test Conditions

The experimental validation was performed using a dedicated double-pulse test setup designed to characterize the switching behaviour of the investigated IGBT modules under operating conditions representative of the target inverter application.

The maximum test conditions were selected according to the protection limits of the industrial inverter platform in which the devices are intended to operate [20]. In particular, the inverter protection thresholds are:

$$V_{DC,max} = 1250\ V$$

$$I_{AC,max} = 1100\ A_{pk}$$

These limits were used to define the maximum admissible test conditions while maintaining safe operation of both the semiconductor devices and the test equipment.

For the experimental characterization, the reference operating point specified in the Infineon datasheet for the FS450R17OE4 module was selected [8]:

$$V_{DC} = 900\ V$$

$$I_C = 450\ A$$

where the current refers to a single IGBT module.

The switching tests were performed under two different thermal conditions:

- Room temperature.
- Elevated temperature with the module baseplate maintained at $125°C$.

These operating conditions allow the influence of temperature on switching losses and transient behaviour to be evaluated.
Throughout the testing campaign, all measurements were performed within the maximum ratings and safe operating areas specified by the manufacturer. Particular attention was devoted to compliance with the Reverse Bias Safe Operating Area (RBSOA) of the IGBT and the corresponding safe operating limits of the freewheeling diode.
A test was considered successful when the collector-emitter voltage measured during switching transients remained below the device blocking voltage rating of 1700 V, even under the most demanding voltage and current conditions.

4.1.2 Double-Pulse Test Method

The switching characterization was performed using the well-established Double-Pulse Test (DPT) technique, which is widely adopted for the evaluation of power semiconductor switching behaviour [19].
The test circuit consists of a DC voltage source, a DC-link capacitor bank, an inductive load, and the device under test (DUT). The load inductance is connected between the inverter phase output and the positive or negative DC bus, depending on whether the upper or lower switch is being characterized.
The device under test is driven using a double-pulse gate signal. The first pulse is used to establish the desired current level within the inductive load, while the second pulse generates the switching transient to be analysed.

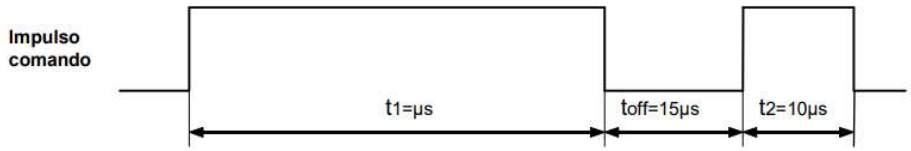

Figure 4.3: Gate drive signal used during the Double-Pulse Test. The first pulse establishes the desired current level in the inductive load, while the second pulse generates the switching transient under investigation.

As shown in Fig. 4.3, the duration of the first pulse t_1 is adjusted according to the desired test current. During this interval, energy is stored in the load inductance and the current increases until the target operating point is reached. After a short off-time interval t_{off}, a second pulse of duration t_2 is applied. This second pulse generates the switching event used for the characterization of the device. The collector-emitter voltage and collector current waveforms are measured during this interval in order to evaluate the dynamic behaviour of the semiconductor.
The Double-Pulse Test allows accurate measurement of:

- Collector-emitter voltage (V_{CE}).
- Collector current (I_C).
- Turn-on energy (E_{on}).
- Turn-off energy (E_{off}).
- Diode reverse recovery energy (E_{rec}).

By properly selecting the DC-link voltage and the duration of the first pulse, switching measurements can be performed at different operating points while maintaining full control of the test conditions.

Current Paths During the Double-Pulse Test

The Double-Pulse Test allows the switching behaviour of both the upper and lower IGBT of the inverter leg to be characterized [19]. During the test, the current follows different conduction paths depending on the switching state of the devices.

Lower IGBT (N-switch) characterization Initially, both IGBTs are turned off and no current flows through the circuit.
During the first pulse t_1, the lower IGBT is turned on while the upper IGBT remains off. The current starts increasing through the load inductance and flows through the lower IGBT.
At the end of the first pulse, the lower IGBT is turned off. During the off-time interval t_{off}, the inductive current cannot change instantaneously and is therefore transferred to the freewheeling diode of the upper switch.
When the second pulse t_2 is applied, the lower IGBT is turned on again. The current commutates from the upper freewheeling diode back to the lower IGBT. During this transition, the reverse recovery behaviour of the diode can be observed and measured.

Upper IGBT (P-switch) characterization A similar procedure is used to characterize the upper IGBT.
Initially, both devices are turned off and no current flows.
During the first pulse t_1, the upper IGBT is turned on and the current increases through the inductive load.
When the upper IGBT is switched off, the current is transferred to the freewheeling diode of the lower switch during the interval t_{off}.
The second pulse t_2 turns the upper IGBT on again, forcing the current to commutate from the lower freewheeling diode back to the upper IGBT. This

transition generates the diode reverse recovery phenomenon and allows the corresponding switching energy to be evaluated.
The different current paths occurring during the Double-Pulse Test are fundamental for the characterization of turn-on energy (E_{on}), turn-off energy (E_{off}), and diode reverse recovery energy (E_{rec}).

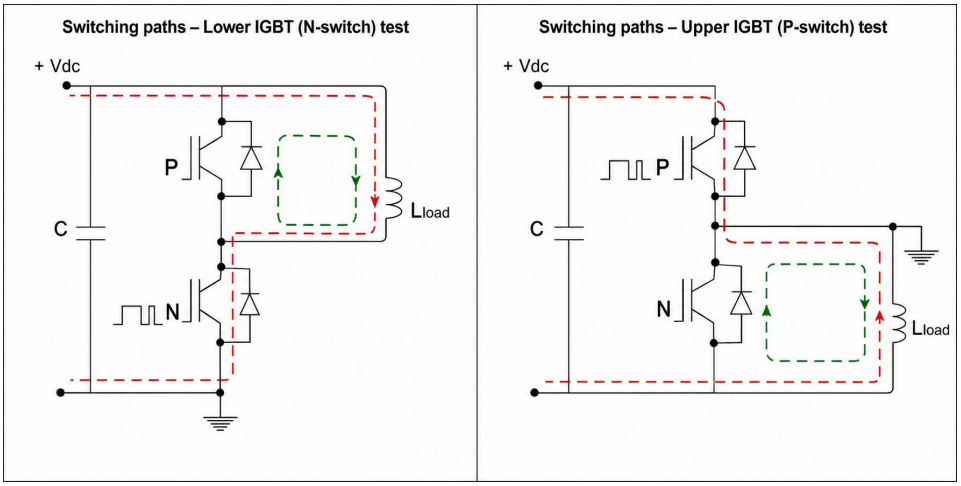

Figure 4.4: Current paths during the double-pulse test for upper and lower switch characterization.

4.1.3 Dead-Time Determination

The turn-on and turn-off delays of both upper and lower IGBTs were experimentally measured under worst-case operating conditions [20].
The minimum required dead-time was estimated from the difference between the measured turn-off and turn-on delays, resulting in values of approximately 2.1–2.2 μs.
To guarantee safe operation under all operating conditions and component tolerances, a dead-time of 6.0 $\pm$ 0.5 μs was adopted during the experimental campaign.

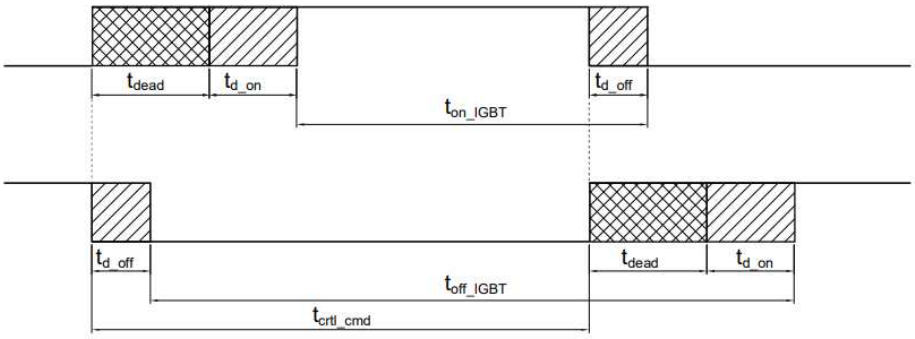

Figure 4.5: Definition of control command, dead-time and IGBT switching delays used for dead-time selection.

t_{ctrl_cmd} Command pulse duration

t_{dead} Dead-time

$t_{d,on}$ IGBT turn-on delay (TPIL40A board + IGBT gate)

$t_{d,off}$ IGBT turn-off delay (TPIL40A board + IGBT gate)

$t_{on,IGBT}$ IGBT ON-state duration

$t_{off,IGBT}$ IGBT OFF-state duration

4.2 Waveform Analysis

Representative switching waveforms acquired during the experimental campaign are reported in Figures 4.6 and 4.7 [20].
For both figures, the measured quantities are represented using the following colour convention:

- **Blue waveform**: collector-emitter voltage V_{CE} (200 V/div);
- **Cyan waveform**: gate-emitter voltage V_{GE} (5 V/div);
- **Magenta waveform**: collector current measured through the Rogowski probe (100 mV/div);
- **Green waveform**: total load current I_C (200 mV/div).

The analysis of these waveforms provides a deeper understanding of the dynamic behaviour of the FS450R17OE4 module and allows the main physical phenomena occurring during switching transitions to be identified.

4.2.1 Turn-On Transient

Initially, the IGBT is in the blocking state and the entire DC-link voltage appears across the device. As soon as the gate voltage starts increasing, the device enters the active region and the collector current begins to rise.
A clear Miller plateau can be observed on the gate voltage waveform. During this interval, the gate current is mainly employed to charge the Miller capacitance (C_{GC}), while the collector-emitter voltage rapidly decreases from the DC-link value towards the on-state voltage.
At the end of the voltage transition, the IGBT reaches its fully enhanced state and the collector current is completely transferred from the freewheeling diode to the semiconductor device.

The measured current waveform also exhibits a transient overshoot caused by parasitic inductances and reverse recovery effects associated with the complementary diode. Such phenomena are unavoidable in practical high-power converter implementations and become more significant when high current gradients are involved.

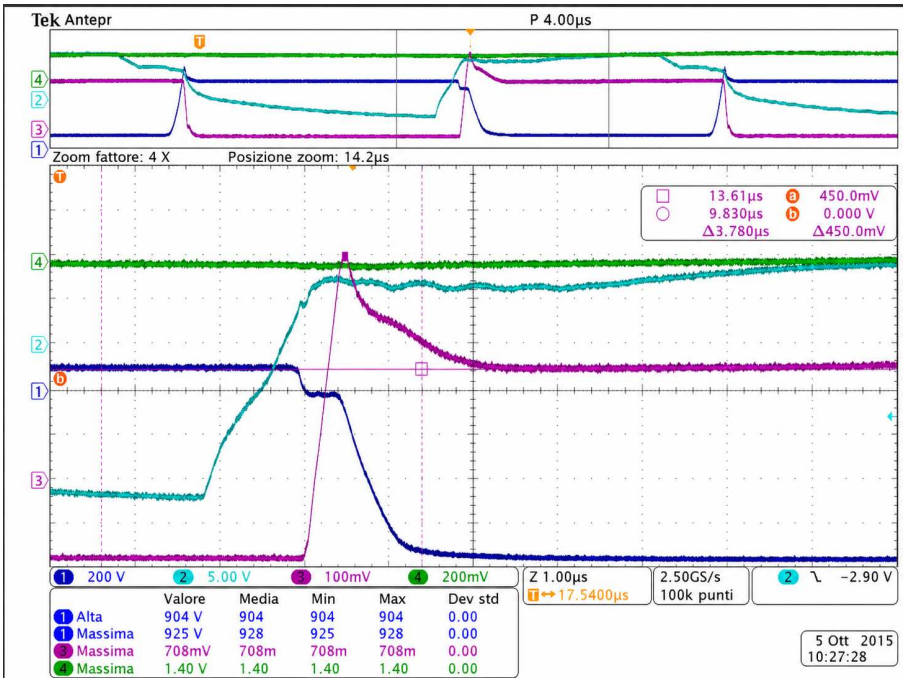

Figure 4.6: Experimental turn-on switching waveforms of the FS450R17OE4 module.

4.2.2 Turn-Off Transient

When the gate command is removed, the gate-emitter voltage starts decreasing and reaches the Miller plateau region. During this interval, the collector-emitter voltage increases until the complete blocking capability of the device is restored.

Simultaneously, the collector current commutates from the IGBT to the free-wheeling diode. Due to the presence of unavoidable stray inductances within the commutation loop, a voltage overshoot can be observed during the transition.

Nevertheless, the measured peak voltage always remains below the maximum allowable device voltage rating of 1700 V, thus confirming the safe operation of the converter under all investigated operating conditions.

After the switching transient, the collector current becomes negligible and the device returns to the off-state condition, sustaining the full DC-link voltage.

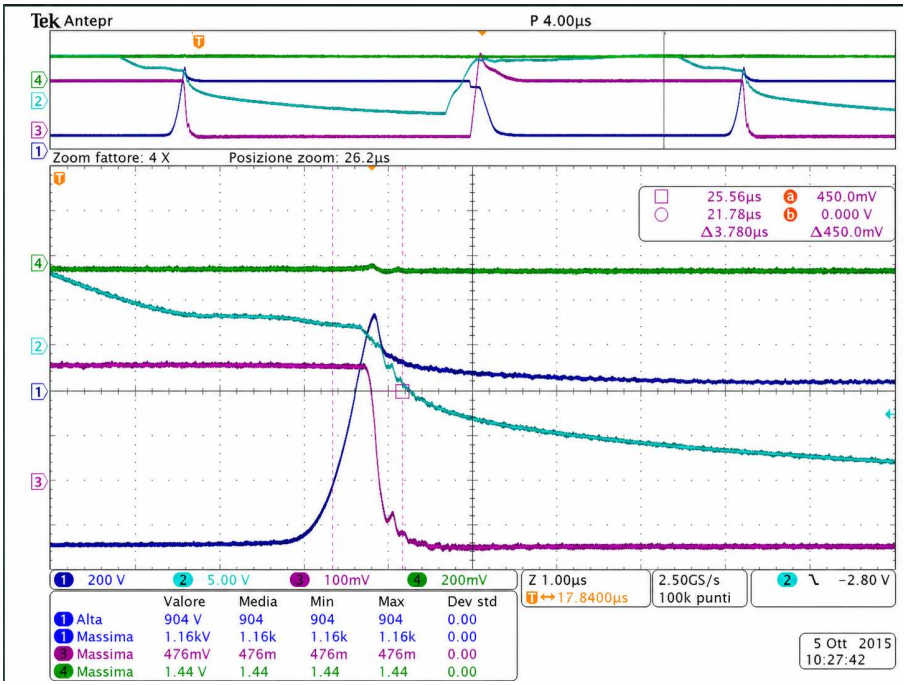

Figure 4.7: Experimental turn-off switching waveforms of the FS450R17OE4 module.

4.2.3 Discussion

The acquired waveforms confirm the expected switching behaviour of the FS450R17OE4 module and clearly highlight the main physical phenomena associated with high-power IGBT commutation, including the Miller effect, reverse recovery phenomena, current overshoots, and voltage transients.

The measured waveforms also demonstrate the correct operation of both the gate driver architecture and the adopted protection strategy under the investigated operating conditions. The nearly constant value of the total load current during the switching transient confirms the typical operating principle of the double pulse test, where the current is assumed to remain approximately constant during the short commutation interval. A more detailed comparison between the experimentally measured switching energies and the manufacturer datasheet values, together with a discussion of the influence of the experimental setup parasitic elements, is presented in the following section.

4.3 Results and Comparison with Datasheet

A direct comparison between the experimental measurements and the MATLAB electro-thermal model is not straightforward.
The developed MATLAB tool performs a continuous-time electro-thermal simulation of a complete three-phase inverter operating under steady-state conditions, where semiconductor losses are continuously evaluated over several fundamental periods.
Conversely, the experimental campaign was based on a double pulse test (DPT), which allows the characterization of the switching behaviour of the semiconductor during a single switching event under controlled operating conditions.
For this reason, a direct comparison between simulated and measured switching energies would not be fully representative.
Instead, the experimental results were compared against the switching energy values reported in the manufacturer datasheet under equivalent operating conditions. Since the MATLAB model itself is entirely based on the interpolation of datasheet curves, an agreement between measurements and datasheet values indirectly validates the adopted modelling approach.
The comparison was performed at a collector-emitter voltage of 900 V and a baseplate temperature of 125°C, corresponding to the conditions adopted during the experimental campaign.
The gate resistance values used during the tests differ from the nominal datasheet conditions because three FS450R17OE4 modules are connected in parallel and driven by the same gate driver unit [20]. Consequently, the gate current supplied by the driver is shared among the three modules.
As shown in Figure 4.1, the contribution of the resistances located on the TPIL40A board was referred to the single device by multiplying their values by three. The local resistances mounted on the GPG3A protection board were then added to obtain the effective gate resistance seen by each IGBT.

$$R_{g,on} = 3R_{TPIL,on} + R_{GPG,on} + R \tag{4.1}$$

$$R_{g,on} = 3 \cdot 0.5 + 3.3 + 0.2 = 5\ \Omega \tag{4.2}$$

$$R_{g,off} = 3R_{TPIL,off} + R_{GPG,off} + R \tag{4.3}$$

$$R_{g,off} = 3 \cdot 3.3 + 10 + 0.2 = 20.1\ \Omega \tag{4.4}$$

Figure 4.8 reports the dependence of the switching energies on the gate resistance according to the FS450R17OE4 datasheet [8]. The experimentally determined gate resistance values were used to interpolate the corresponding datasheet energies and perform the comparison with the measured results.

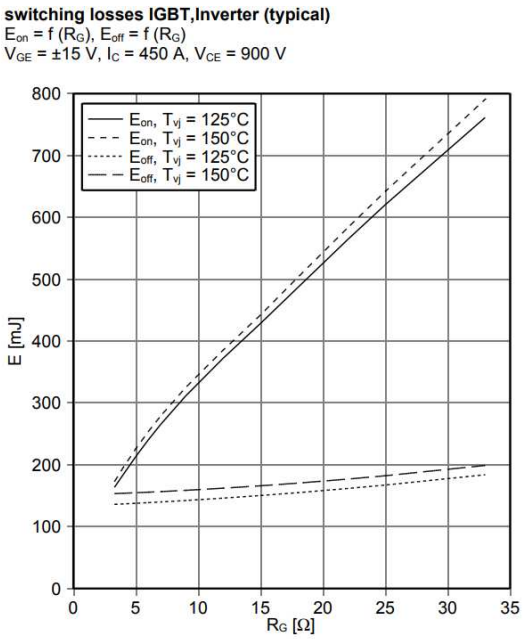

Figure 4.8: Dependence of switching energies on gate resistance according to the FS450R17OE4 datasheet ($V_{CE} = 900$ V, $I_C = 450$ A).

Table 4.1: Comparison between measured and datasheet switching energies at $V_{CE} = 900$ V, $I_C = 450$ A and $T_C = 125°C$

Parameter	Measured	Datasheet	Deviation [%]
E_{on} [mJ]	323–344	215	+50–60
E_{off} [mJ]	207–234	160	+29–46

Although the experimental switching energies are higher than the corresponding datasheet values, this difference can be reasonably explained by the different test setups adopted.

The switching energy values reported in the FS450R17OE4 datasheet are obtained under well-defined laboratory conditions, including a commutation stray inductance equal to only 35 nH and a turn-on current slope of approximately 4800 A/μs [8].

Conversely, the experimental setup developed in this work consists of a complete industrial test bench, including busbars, protection boards, gate driver boards, measurement probes and external connections, all contributing additional parasitic inductances [20].

The measured current slopes during the experimental campaign ranged between approximately 1450 A/μs and 1700 A/μs during turn-on, which is sig-

nificantly lower than the value specified in the datasheet [20, 8]. This observation suggests that the overall commutation loop inductance of the experimental setup is considerably higher than that adopted by Infineon during device characterization.
Since the exact layout and parasitic elements of the manufacturer test bench are not disclosed, a direct quantitative comparison is not fully possible. Nevertheless, the measured energies remain of the same order of magnitude as the datasheet values, confirming the overall validity of both the experimental procedure and the adopted modelling approach.

Chapter 5

Cost Analysis and Economic Considerations

Besides the electrical and thermal performance improvements discussed in the previous sections, the economic impact of the proposed solutions must also be considered.
Particular attention was dedicated to evaluating the feasibility of adopting Silicon Carbide (SiC) technology and to estimating the cost reduction achievable through the introduction of a more integrated inverter architecture.

5.0.1 Silicon Carbide Adoption

Silicon Carbide (SiC) MOSFETs represent one of the most promising technologies currently available in power electronics due to their superior switching performance, lower switching losses, and capability of operating at significantly higher switching frequencies compared to conventional silicon devices [7].
The higher switching frequency achievable with SiC devices can allow a reduction in the size of passive components, especially output filters, inductors, capacitors, or isolation transformers. This advantage is particularly relevant in grid-connected converters, where passive filtering elements may represent a significant part of the overall system volume and cost.
However, from an economic point of view, the adoption of SiC MOSFET technology is currently not convenient for the considered marine drive platform. The production cost of the reference AD5W740L drive is approximately 5500 EUR. Within this cost, the power semiconductor modules account for approximately 1000 EUR.
Assuming that the cost of the power modules would increase by a factor of three when replacing the existing IGBT solution with SiC devices, the semiconductor cost would increase from approximately 1000 EUR to 3000 EUR. As a consequence, the total inverter cost would increase from approximately 5500 EUR

to 7500 EUR, corresponding to an additional cost of about 2000 EUR.
This cost increase is higher than the maximum potential saving associated with the reduction of external sinusoidal filters, which is estimated to be approximately 1500 EUR. Therefore, for the specific motor-drive application considered in this thesis, the economic benefit of adopting SiC devices is currently not sufficient to compensate for their higher cost.
In motor-drive applications, the switching frequency does not necessarily need to be significantly increased. For standard industrial and marine propulsion motors, switching frequencies in the range of a few kilohertz are usually sufficient to achieve acceptable current quality and motor control performance. Higher switching frequencies may be justified only in specific cases, such as high-speed machines or motors with a large number of pole pairs, where the fundamental electrical frequency can become very high. For example, if the modulation frequency reaches approximately 600 Hz, the switching frequency should typically be at least twenty times higher, leading to values above 10 kHz. Moreover, the very fast voltage transitions generated by SiC MOSFETs produce high dv/dt values, which can increase the electrical stress applied to motor windings. In inverter-fed motors, steep voltage rise times and high-frequency PWM excitation may overstress the winding insulation and contribute to partial discharge phenomena. Partial discharges are localized dielectric breakdowns that progressively degrade the insulation system through electrical, chemical, and thermal stress, eventually increasing the risk of winding insulation failure [21].
As a consequence, one of the main advantages of SiC technology, namely the possibility of strongly increasing the switching frequency and reducing passive component size, cannot be fully exploited in the considered application without introducing additional system-level constraints.
For these reasons, SiC technology is considered a promising future development rather than the most suitable short-term solution for the investigated AD5W740L marine drive. A future reduction in SiC device cost may improve the economic balance and make this technology more attractive also for high-power marine motor-drive applications.

5.0.2 Gate Driver Integration and Cost Reduction

Additional cost reductions can be achieved through the simplification of the gate driver and protection architecture.
In the current implementation, the three-phase converter uses TPIL46CA gate driver boards together with GPG3A protection boards. Considering the complete three-phase converter, the total cost associated with these boards is ap-

proximately 513 EUR, resulting from 379 EUR for the TPIL46CA gate driver boards and 134 EUR for the GPG3A protection boards. This corresponds to an average cost of approximately 171 EUR per phase.
The future architecture aims to eliminate the separate GPG3A protection boards by integrating the protection functionalities directly into a single gate driver unit mounted on each LV100 power module, as discussed in Chapter 2. The target cost of the new integrated board is approximately 100 EUR per phase.
Therefore, the total cost of the present solution is:

$$C_{\text{current}} = 379 + 134 = 513 \text{ EUR} \tag{5.1}$$

while the expected cost of the proposed integrated solution is:

$$C_{\text{new}} = 3 \times 100 = 300 \text{ EUR} \tag{5.2}$$

The resulting estimated saving is therefore:

$$\Delta C = 513 - 300 = 213 \text{ EUR} \tag{5.3}$$

per converter.
Besides the direct economic benefit, the integration of gate driver and protection functionalities also reduces wiring complexity, assembly effort, occupied volume, and the number of interconnections. This contributes to improving converter manufacturability, maintainability, and overall system reliability.

Chapter 6

Conclusions and Future Developments

6.1 Conclusions

This thesis investigated the potential evolution of the power semiconductor technology currently adopted in the Nidec ASI AD5000 marine drive platform. The study began with an analysis of the operating principles of voltage source inverters and of the main semiconductor technologies employed in medium- and high-power converters for marine applications. Particular attention was devoted to the role of power devices in determining converter efficiency, thermal behaviour, power density, and overall system performance.

A MATLAB-based electro–thermal simulation tool was then developed to evaluate conduction losses, switching losses, and junction temperatures of different IGBT technologies under realistic operating conditions. The model was implemented using manufacturer datasheet information and was subsequently validated through comparison with both Infineon IPOSIM simulations and experimental measurements obtained by means of double pulse tests performed on the existing EconoPACK+ solution.

The good agreement observed between simulations, datasheet values, and experimental measurements confirmed the validity of the developed modelling approach and allowed the tool to be confidently employed for the comparative analysis of alternative semiconductor technologies.

The comparison between the currently adopted FS450R17OE4 modules and the new generation LV100 IGBT devices demonstrated that the latest technology provides significant advantages in terms of power density and electrical performance. In particular, the new devices allow either a reduction of semiconductor losses at the same operating current or, alternatively, an increase of the output current while maintaining comparable loss levels. The performed

analyses showed that the converter current capability could potentially be increased from 680 A to approximately 800 A without introducing additional thermal stress on the semiconductor devices.
Furthermore, the adoption of the LV100 package enables a considerable reduction in converter dimensions, simplifying the overall architecture and contributing to a reduction in auxiliary electronics, wiring complexity, and manufacturing costs.
Overall, the obtained results demonstrate that the transition towards new-generation LV100 IGBT technology represents a feasible and attractive solution for future developments of the AD5000 marine drive platform.

6.2 Future Developments

Several possible developments can be identified as a continuation of the present work.
First, further experimental validation activities should be performed once the new LV100-based prototype becomes available. Experimental characterization under real operating conditions would allow the simulation results presented in this work to be fully validated and would provide additional information regarding long-term reliability and thermal behaviour.
Another possible improvement concerns the extension of the developed MATLAB tool. Additional functionalities, such as lifetime estimation, reliability analysis, and detailed electro-magnetic modelling, could be integrated in order to provide a more comprehensive evaluation of converter performance.
Finally, Silicon Carbide (SiC) MOSFET technology represents one of the most promising future research directions. Owing to their superior switching characteristics, SiC devices could further reduce switching losses, increase converter efficiency, and enable operation at significantly higher switching frequencies. The resulting reduction in passive component size could lead to additional improvements in power density and overall system compactness.
Although the present study did not consider the implementation of SiC technology because of its higher cost and the limited industrial experience available in marine applications, future reductions in semiconductor cost and further improvements in device reliability may make SiC MOSFETs an attractive alternative for next-generation marine propulsion converters.

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Appendix A

MATLAB Simulation Code

The MATLAB software developed during this thesis was used to evaluate the electrical and thermal behaviour of different power semiconductor technologies under operating conditions representative of the AD5000 marine drive platform. The complete simulation framework includes several files containing the electrical and thermal parameters of the investigated devices, together with dedicated routines for loss calculation and thermal analysis. For brevity, only the main simulation script and the core functions implementing the electro-thermal model are reported in this appendix. Device-specific files containing datasheet-derived lookup tables are not included since they mainly consist of numerical parameters extracted from manufacturers' datasheets.

A.1 Main Simulation Script

The following listing reports the main MATLAB script responsible for waveform generation, loss calculation, thermal network solution, and post-processing of simulation results.

```
%file principale ultimo aggiornamento 18/12/2025

clear
clc
close all

% Load device data

FS450R17KE4_FLAG = 0; %Old one 450A need parallelization
FS450R17OE4_FLAG  = 1;
FF1200XTR17T2P5_FLAG  = 0; %1200A available
FF1400R17T2P8_FLAG  = 0; % newest gen8 1400A (not available yet)

flags = [FF1200XTR17T2P5_FLAG , FS450R17KE4_FLAG , FS450R17OE4_FLAG ,
    FF1400R17T2P8_FLAG ];

if sum(flags) ~= 1
    error('Selezione device non valida: attivare UNA sola flag alla volta.');
end
```

```
19
20 %% Simulation parameters
21
22 Vdc         = 1110;          % DC bus voltage [V]
23 ma          = 1.0;           % Modulation index
24 f           = 50;            % Output frequency [Hz]
25 f_sw        = 4000;          % Switching frequency [Hz]
26 I_RMS_base  = 680;           % RMS "totale" che vuoi inserire tu
27 cosphi      = 0.8;           % Power factor
28 Periods     = 300;           % Number of fundamental periods
29 T_step      = 0.5e-6;        % Simulation time step [s]
30 T_heatsink = 60;            % Heatsink temperature [ C ]
31 FILTER_K    = 2e-6;          % IIR filter coefficient for thermal power
32 I_RMS = I_RMS_base;         % default
33
34
35
36 if FF1200XTR17T2P5_FLAG
37     load FF1200XTR17T2P5
38     fprintf('Device simulated : FF1200XTR17T2P5 ');
39     Rgon  = 0.5; %default value
40     Rgoff = 4.5; %default value
41 end
42
43
44 if FS450R17KE4_FLAG
45     load FS450R17KE4
46     fprintf('Device simulated : FS450R17KE4 ');
47     I_RMS =  I_RMS_base/3;  %parallelizzati
48     Rgon  = 3.3; %default value
49     Rgoff = 3.3; %default value
50     Rgon_table  = 0;
51     Rgoff_table = 0;
52     Rgrec_table = 0;
53     k_Rgon  = (-0.2276/(Rgon/3.3 - 0.52214) + 0.393902*(Rgon/3.3) + 1.0824);
54     k_Rgoff = ( 0.391569/(Rgoff/3.3 + 1.387072) + 0.057981*(Rgoff/3.3) +
           0.77874);
55     %Diode recovery occurs when the opposite IGBT turns ON
56     k_Rgrec = (1.383939/(Rgon/3.3 + 1.360003)-0.01503*(Rgon/3.3) + 0.431418);
57 end
58
59 if FS450R17OE4_FLAG
60     load FS450R17OE4
61     fprintf('Device simulated : FS450R17OE4 ');
62     I_RMS =  I_RMS_base/3;  %parallelizzati
63     Rgon  = 3.3; %default value
64     Rgoff = 3.3; %default value
65     Rgon_table  = 0;
66     Rgoff_table = 0;
67     Rgrec_table = 0;
68     k_Rgon  = (-1.06062881674435/(Rgon/3.3+0.806577825475071)
           +0.353580575843822*(Rgon/3.3)+1.22960609504316);
69     k_Rgoff = (42.5516819067756/(Rgoff/3.3+23.976609508906)
           +0.0888918924361269*(Rgoff/3.3)+-0.793088822028427);
70     %Diode recovery occurs when the opposite IGBT turns ON
71     k_Rgrec = (1.36803224005115/(Rgon/3.3+1.52626050986323)
           +-0.016324159048855*(Rgon/3.3)+0.474109657251298);
72 end
73
74 if FF1400R17T2P8_FLAG
```

```
    load FF1400R17T2P8
    fprintf('Device simulated : FF1400R17T2P8 ');
    Rgon  = 0.7; %default value
    Rgoff = 9.3; %default value
    Rgrec = 0.7; %default value
    Rgon_table  = 0;
    Rgoff_table = 0;
    Rgrec_table = 0;
    k_Rgon  = 1;
    k_Rgoff = 1;
    k_Rgrec = 1;
end

fprintf('\nSimulation Parameter : Vdc = %g V | I_RMS = %g A | f_sw = %g Hz \n'
    , Vdc, I_RMS, f_sw);
%% Electrical waveforms

phi   = acos(cosphi);
Vac   = sqrt(3)*ma*(Vdc/2)/sqrt(2);     % Line RMS voltage [V]
T     = 1/f;
T_sim = Periods * T;

t = 0:T_step:T_sim;

I = sqrt(2) * I_RMS * cos(2*pi*f*t - phi);

V_tri = sawtooth(2*pi*f_sw*t - pi/2, 1/2);
V_sin = ma * cos(2*pi*f*t);

% PWM generation
states = (V_sin >= V_tri);
V      = (Vdc/2) * (2*states - 1);

P_load = sqrt(3) * Vac * I_RMS * cosphi;

%% Loss energy initialization

N = length(t);

E_loss_cond_Q1   = zeros(1,N);
E_loss_switch_Q1 = zeros(1,N);
E_loss_cond_D1   = zeros(1,N);
E_loss_switch_D1 = zeros(1,N);

E_loss_cond_Q2   = zeros(1,N);
E_loss_switch_Q2 = zeros(1,N);
E_loss_cond_D2   = zeros(1,N);
E_loss_switch_D2 = zeros(1,N);

%% Thermal model parameters

Rch_VEC = [RthCH_IGBT, Rthch_Diode, RthCH_IGBT, Rthch_Diode];

R_MAT = [Rth_IGBT_JC;
    Rth_Diode_JC;
    Rth_IGBT_JC;
    Rth_Diode_JC];      % Q1, D1, Q2, D2

Tau_MAT = [tauth_IGBT_JC;
    tauth_Diode_JC;
```

```
    tauth_IGBT_JC;
    tauth_Diode_JC];

C_MAT = Tau_MAT ./ R_MAT;    % Thermal capacitances (C = tau / R)

dT_RC  = zeros(4,4);
Tj_VEC = [102; 83; 102; 83]; % Initial junction temperatures [ C ]

P_Old_VEC          = zeros(4,1);
P_Old_VEC_filtered = zeros(4,1);

%% Logging variables

Tj_history  = zeros(4,N);
dT_CH_array = zeros(4,N);

state_old = 1;   % 1 = high-side ON, 0 = low-side ON

comm_cntr = zeros(1,4);

Q1 = 1; D1 = 2; Q2 = 3; D2 = 4;

%% Main simulation loop

for i = 1:N

    % Instantaneous power vectors
    P_inst_sw   = zeros(1,4);
    P_inst_cond = zeros(1,4);

    I_i     = I(i);
    state_i = V(i) > 0;

    % Store junction temperature history
    Tj_history(:,i) = Tj_VEC;

    if state_i == 1
        % -------- High-side ON --------
        if I_i >= 0
            % Quadrant 1: Q1 conduction
            V_i = Voltage_calc(T_table, I_IGBT_conduction_table, ...
                V_IGBT_conduction_table, abs(I_i), Tj_VEC(Q1));
            E_loss_cond_Q1(i) = T_step * V_i * abs(I_i);

            if state_i ~= state_old
                comm_cntr(Q1) = comm_cntr(Q1) + 1;

                E_loss_switch_Q1(i) = energy_calc(Rgon_table, k_Rgon, ...
                    I_IGBT_switching_table, E_on, T_table, V_ref_E_loss, ...
                    Rgon, abs(I_i), Tj_VEC(Q1), Vdc);

                E_loss_switch_D2(i) = energy_calc(Rgrec_table, k_Rgrec, ...
                    I_Diode_switching_table, E_rec, T_table, V_ref_E_loss, ...
                    Rgon, abs(I_i), Tj_VEC(D2), Vdc);
            end
        else
            % Quadrant 4: D1 conduction
            V_i = Voltage_calc(T_table, I_Diode_conduction_table, ...
                V_Diode_conduction_table, abs(I_i), Tj_VEC(D1));
            E_loss_cond_D1(i) = T_step * V_i * abs(I_i);
```

```
194
195             if state_i ~= state_old
196                 comm_cntr(D1) = comm_cntr(D1) + 1;
197                 E_loss_switch_Q2(i) = energy_calc(Rgoff_table, k_Rgoff, ...
198                     I_IGBT_switching_table, E_off, T_table, V_ref_E_loss, ...
199                     Rgoff, abs(I_i), Tj_VEC(Q2), Vdc);
200             end
201         end
202     else
203         % -------- Low-side ON --------
204         if I_i >= 0
205             % Quadrant 2: D2 conduction
206             V_i = Voltage_calc(T_table, I_Diode_conduction_table, ...
207                 V_Diode_conduction_table, abs(I_i), Tj_VEC(D2));
208             E_loss_cond_D2(i) = T_step * V_i * abs(I_i);
209
210             if state_i ~= state_old
211                 comm_cntr(Q1) = comm_cntr(Q1) + 1;
212                 E_loss_switch_Q1(i) = energy_calc(Rgoff_table, k_Rgoff, ...
213                     I_IGBT_switching_table, E_off, T_table, V_ref_E_loss, ...
214                     Rgoff, abs(I_i), Tj_VEC(Q1), Vdc);
215             end
216         else
217             % Quadrant 3: Q2 conduction
218             V_i = Voltage_calc(T_table, I_IGBT_conduction_table, ...
219                 V_IGBT_conduction_table, abs(I_i), Tj_VEC(Q2));
220             E_loss_cond_Q2(i) = T_step * V_i * abs(I_i);
221
222             if state_i ~= state_old
223                 comm_cntr(Q2) = comm_cntr(Q2) + 1;
224
225                 E_loss_switch_D1(i) = energy_calc(Rgrec_table, k_Rgrec, ...
226                     I_Diode_switching_table, E_rec, T_table, V_ref_E_loss, ...
227                     Rgon, abs(I_i), Tj_VEC(D1), Vdc);
228
229                 E_loss_switch_Q2(i) = energy_calc(Rgon_table, k_Rgon, ...
230                     I_IGBT_switching_table, E_on, T_table, V_ref_E_loss, ...
231                     Rgon, abs(I_i), Tj_VEC(Q2), Vdc);
232             end
233         end
234     end
235
236     % Instantaneous powers
237     E_sw   = [E_loss_switch_Q1(i), E_loss_switch_D1(i), ...
238         E_loss_switch_Q2(i), E_loss_switch_D2(i)] / 1000;
239
240     E_cond = [E_loss_cond_Q1(i), E_loss_cond_D1(i), ...
241         E_loss_cond_Q2(i), E_loss_cond_D2(i)];
242
243     P_inst_sw   = E_sw   / T_step;
244     P_inst_cond = E_cond / T_step;
245
246
247     % Total instantaneous power vector
248     P_inst_TOT = P_inst_sw + P_inst_cond;
249     p_inst_VEC = P_inst_TOT';
250
251     % Power filtering for thermal model
252     P_Old_VEC_filtered = P_Old_VEC*FILTER_K + ...
253         P_Old_VEC_filtered*(1 - FILTER_K);
```

```
254
255     % Case-to-heatsink temperature rise
256     dT_CH = P_Old_VEC_filtered .* Rch_VEC';
257     dT_CH_array(:,i) = dT_CH;
258
259     % Junction-to-case RC network update
260     P_old_EXP = repmat(P_Old_VEC, 1, 4);
261     dT_RC = dT_RC + ...
262         (P_old_EXP - dT_RC ./ R_MAT) .* ...
263         (T_step ./ C_MAT);
264
265     % Junction temperature update
266     T_case = T_heatsink + dT_CH;
267     Tj_VEC = T_case + sum(dT_RC, 2);
268
269     P_Old_VEC = p_inst_VEC;
270     state_old = state_i;
271
272 end
273
274 %% Post-processing and plots
275 figure(1)
276 % Plot Q1 (Riga 1)
277 subplot(2,1,1)
278 plot(t, Tj_history(1, :), 'r', 'LineWidth', 1.5);
279 hold on;
280 % Plot D1 (Riga 2)
281 plot(t, Tj_history(2, :), 'b', 'LineWidth', 1.5);
282 title('Temperature High-Side (Q1 & D1)');
283 legend('IGBT Q1', 'Diode D1');
284 xlabel('Tempo [s]'); ylabel('Tj [ C ]');
285 grid on;
286
287 % Plot Q2 (Riga 3) e D2 (Riga 4)
288 subplot(2,1,2)
289 plot(t, Tj_history(3, :), 'r--', 'LineWidth', 1.5);
290 hold on;
291 plot(t, Tj_history(4, :), 'b--', 'LineWidth', 1.5);
292 title('Temperature Low-Side (Q2 & D2)');
293 legend('IGBT Q2', 'Diode D2');
294 xlabel('Tempo [s]'); ylabel('Tj [ C ]');
295 grid on;
296
297
298 figure(2)
299 plot(dT_CH_array');
300 xlabel('Time [s]', 'FontSize', 12)
301 ylabel(' T_ {case-heatsink} [ C ]', 'FontSize', 12)
302
303 %% ------------------- Steady-state calculation -------------------
304
305 % Steady-state window: last 1 period
306 steady_mask = t >= (t(end) - T);   % time mask
307
308 %% Steady-state average powers
309
310 % Conduction losses
311 P_loss_cond_Q1 = sum(E_loss_cond_Q1(steady_mask)) / T;
312 P_loss_cond_D1 = sum(E_loss_cond_D1(steady_mask)) / T;
313 P_loss_cond_Q2 = sum(E_loss_cond_Q2(steady_mask)) / T;
```

```
P_loss_cond_D2 = sum(E_loss_cond_D2(steady_mask)) / T;

% Switching losses (from mJ to J)
P_loss_switch_Q1 = sum(E_loss_switch_Q1(steady_mask)) / 1000 / T;
P_loss_switch_D1 = sum(E_loss_switch_D1(steady_mask)) / 1000 / T;
P_loss_switch_Q2 = sum(E_loss_switch_Q2(steady_mask)) / 1000 / T;
P_loss_switch_D2 = sum(E_loss_switch_D2(steady_mask)) / 1000 / T;

% Total losses per device
P_tot_Q1 = P_loss_cond_Q1 + P_loss_switch_Q1;
P_tot_D1 = P_loss_cond_D1 + P_loss_switch_D1;
P_tot_Q2 = P_loss_cond_Q2 + P_loss_switch_Q2;
P_tot_D2 = P_loss_cond_D2 + P_loss_switch_D2;

%% Steady-state average/min/max junction temperatures

Tj_mean = mean(Tj_history(:, steady_mask), 2);
Tj_min  = min(Tj_history(:, steady_mask), [], 2);
Tj_max  = max(Tj_history(:, steady_mask), [], 2);

%% Display junction temperatures

names = {'Q1 IGBT','D1 Diode','Q2 IGBT','D2 Diode'};
fprintf('\n--- Junction Temperatures @ steady-state ---\n');
for k = 1:4
    fprintf('%s : Tmean = %.1f  C  | Tmin = %.1f  C  | Tmax = %.1f  C \n', ...
        names{k}, Tj_mean(k), Tj_min(k), Tj_max(k));
end

%% Display device losses

fprintf('\n--- Device losses @ steady-state (last period) ---\n');

fprintf('\nHigh-side:\n');
fprintf('Q1 IGBT : Pcond = %6.1f W | Psw = %6.1f W | Ptot = %6.1f W\n', ...
    P_loss_cond_Q1, P_loss_switch_Q1, P_tot_Q1);
fprintf('D1 Diode: Pcond = %6.1f W | Psw = %6.1f W | Ptot = %6.1f W\n', ...
    P_loss_cond_D1, P_loss_switch_D1, P_tot_D1);

fprintf('\nLow-side:\n');
fprintf('Q2 IGBT : Pcond = %6.1f W | Psw = %6.1f W | Ptot = %6.1f W\n', ...
    P_loss_cond_Q2, P_loss_switch_Q2, P_tot_Q2);
fprintf('D2 Diode: Pcond = %6.1f W | Psw = %6.1f W | Ptot = %6.1f W\n', ...
    P_loss_cond_D2, P_loss_switch_D2, P_tot_D2);

%% Phase and three-phase totals, efficiency

P_phase = P_tot_Q1 + P_tot_D1 + P_tot_Q2 + P_tot_D2;
P_total = 3 * P_phase;

Efficiency = 1 - P_total / P_load;


fprintf('\nTotal phase losses : %.1f W\n', P_phase);
fprintf('Total inverter losses (3-phase): %.1f W\n', P_total);
fprintf('Efficiency: %.3f\n', Efficiency);
```

A.2 Switching Loss Calculation Function

The following function computes the switching energy losses by interpolating the datasheet information as a function of current, temperature, gate resistance, and DC-link voltage.

```
function E_loss = energy_calc(R_array, k_R_map, I_array, E_I_map, ...
                              T_array, V_ref, R_calc, I_calc, T_calc, V_calc)

    % -------- Voltage scaling --------
    k_V = V_calc / V_ref;

    % -------- Energy vs current --------
    tmp_E_I = zeros(1, length(T_array));
    for i = 1:length(T_array)
        tmp_E_I(i) = interp1(I_array, E_I_map(i,:), abs(I_calc), ...
                             'linear', 'extrap');
    end

    % -------- Energy vs temperature --------
    E0 = interp1(T_array, tmp_E_I, T_calc, 'linear', 'extrap');

    % -------- Gate resistance handling --------
    if isscalar(R_array) && R_array == 0
        % Case FS450 or FF1400     no R dependence
        k_R = k_R_map;   % = 1 (or scalar from formula)
    else
        % Case FF1200     R- and T-dependent table
        tmp_k_R = zeros(1, length(T_array));
        for i = 1:length(T_array)
            tmp_k_R(i) = interp1(R_array, k_R_map(i,:), R_calc, ...
                                 'linear', 'extrap');
        end
        k_R = interp1(T_array, tmp_k_R, T_calc, 'linear', 'extrap');
    end

    % -------- Final energy (mJ) --------
    E_loss = E0 * k_R * k_V;
end
```

A.3 Conduction Voltage Interpolation Function

The following routine evaluates the semiconductor conduction voltage through interpolation of the experimentally extracted datasheet curves.

```
function V_calc = Voltage_calc(T_array, I_array, V_map, I_calc, T_calc)
    tmp_V_I = zeros(1,length(T_array));

    for i = 1:length(T_array)
        tmp_V_I(i) = interp1( I_array, V_map(i,:), abs(I_calc));
    end

    V_calc = interp1(T_array, tmp_V_I, T_calc);
end
```